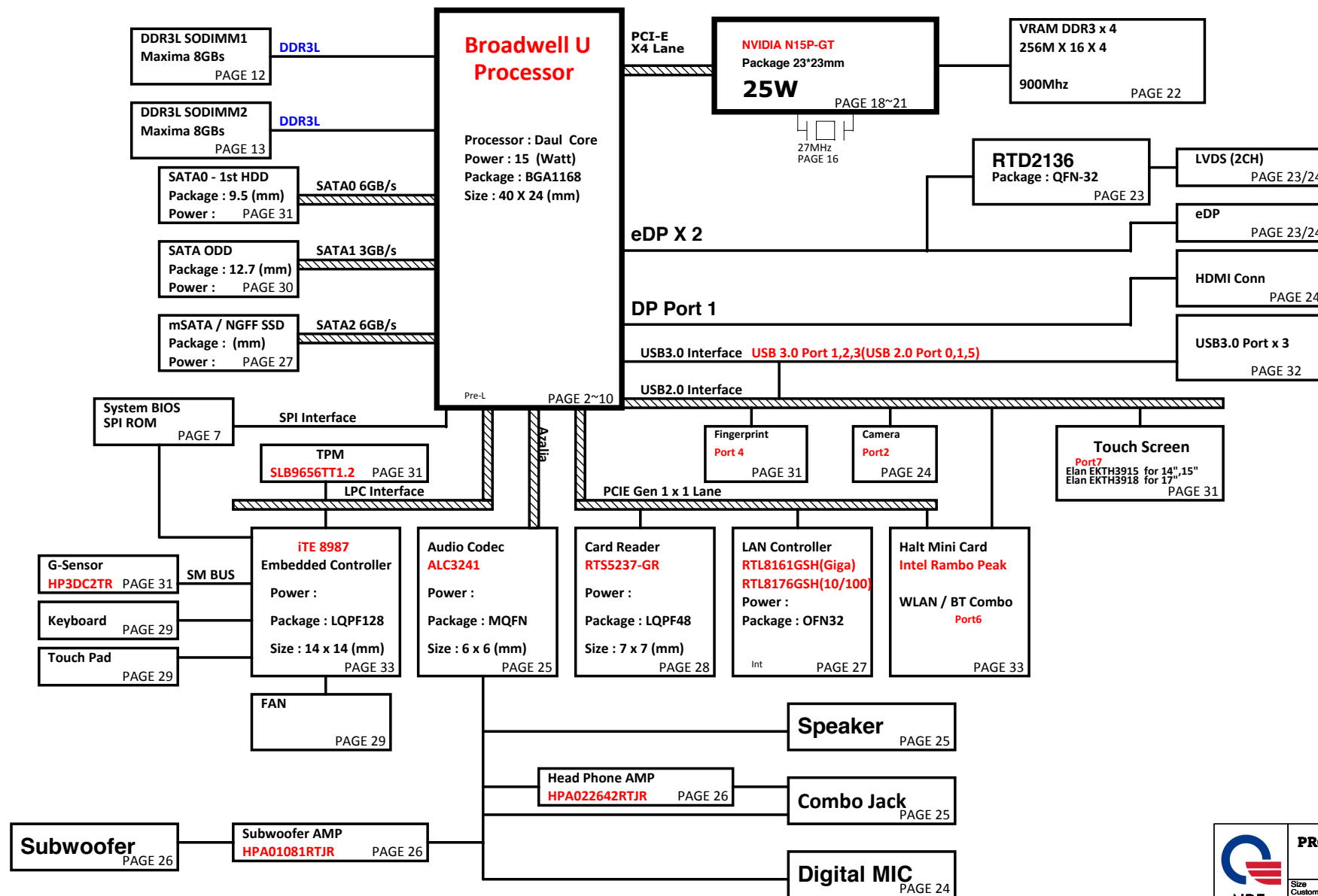
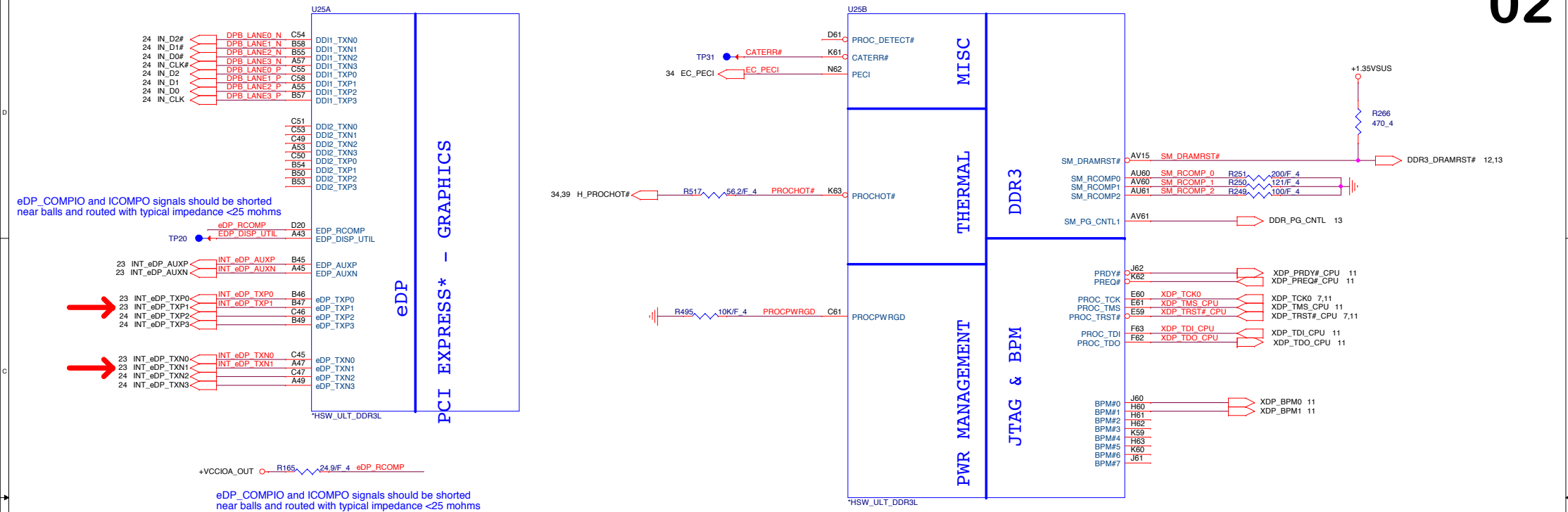


DIS (14" / 15" / 17") S-Vine^{MT} Intel Crescent Bay ULT Platform Block Diagram

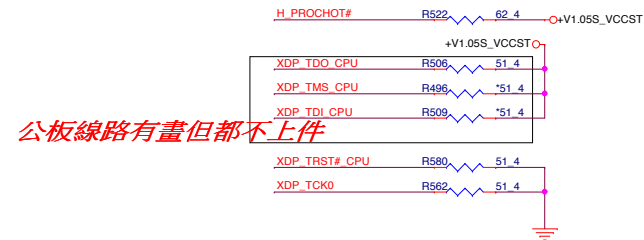
PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

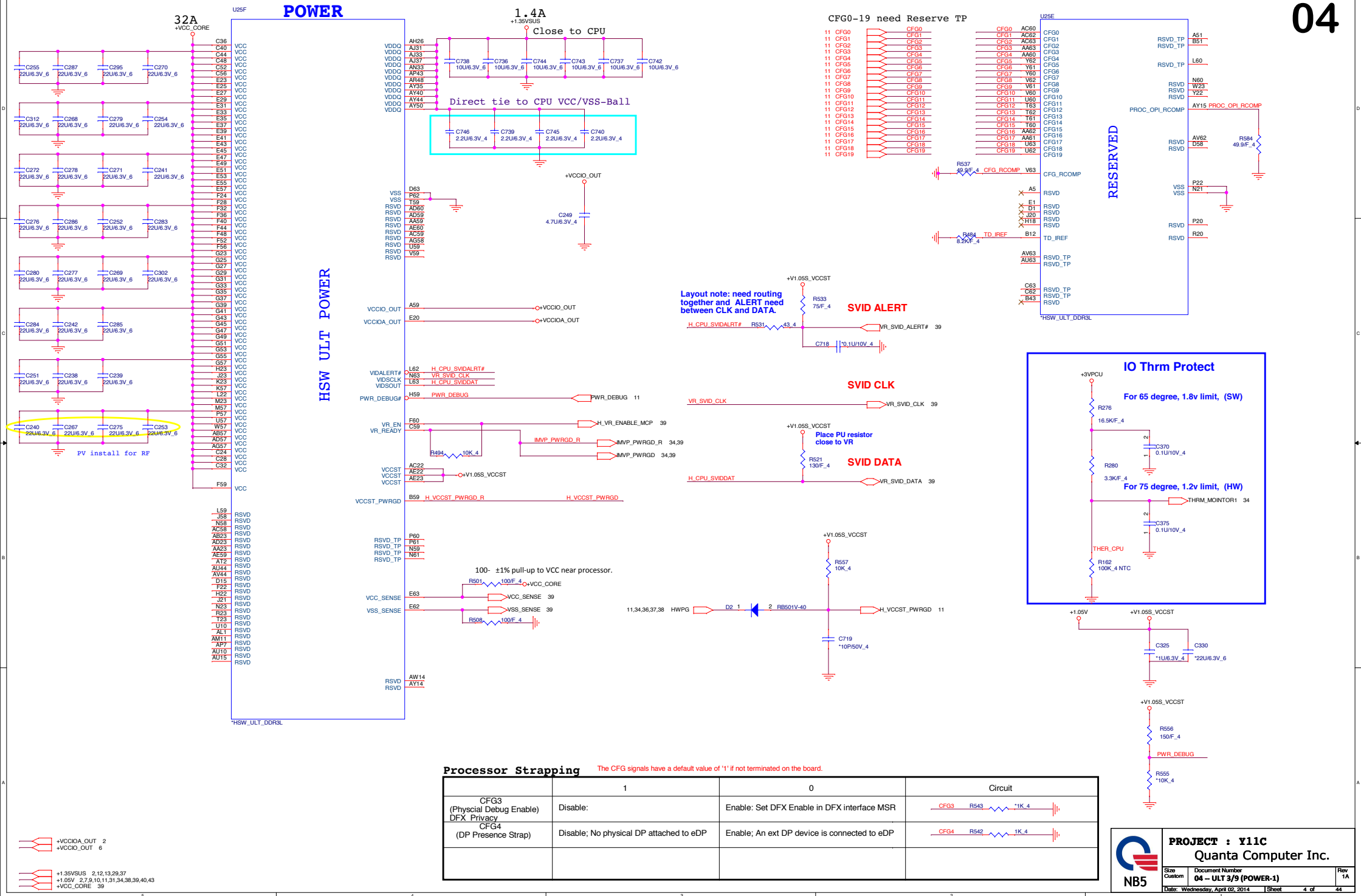




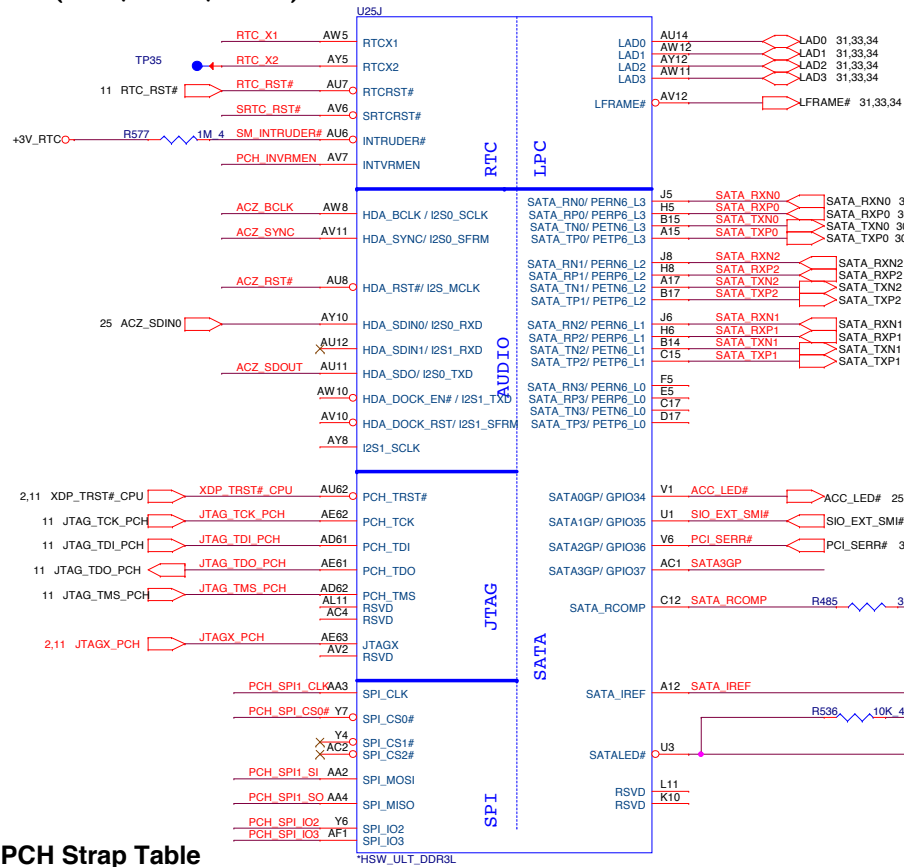
Processor pull-up (CPU)










The diagram illustrates the DDR SYSTEM MEMORY A and B configurations. It includes two main memory blocks, U25C and U25D, each with a detailed pinout and connection list. The U25C block is connected to a 12M A, BS#0, 12M A, BS#1, 12M A, BS#2, 12M A, CAS#, 12M A, RAS#, 12M A, WE#, and 12M A, WE# signals. The U25D block is connected to a 13M B, BS#0, 13M B, BS#1, 13M B, BS#2, 13M B, CAS#, 13M B, RAS#, 13M B, WE#, and 13M B, WE# signals. The U25C block is also connected to a 12M A, VREF, 12M A, VREF, DO0, 12M A, VREF, DO1, 12M A, VREF, DO2, 12M A, VREF, DO3, 12M A, VREF, DO4, 12M A, VREF, DO5, 12M A, VREF, DO6, 12M A, VREF, DO7, 12M A, VREF, DO8, 12M A, VREF, DO9, 12M A, VREF, DO10, 12M A, VREF, DO11, 12M A, VREF, DO12, 12M A, VREF, DO13, 12M A, VREF, DO14, 12M A, VREF, DO15, 12M A, VREF, DO16, 12M A, VREF, DO17, 12M A, VREF, DO18, 12M A, VREF, DO19, 12M A, VREF, DO20, 12M A, VREF, DO21, 12M A, VREF, DO22, 12M A, VREF, DO23, 12M A, VREF, DO24, 12M A, VREF, DO25, 12M A, VREF, DO26, 12M A, VREF, DO27, 12M A, VREF, DO28, 12M A, VREF, DO29, 12M A, VREF, DO30, 12M A, VREF, DO31, 12M A, VREF, DO32, 12M A, VREF, DO33, 12M A, VREF, DO34, 12M A, VREF, DO35, 12M A, VREF, DO36, 12M A, VREF, DO37, 12M A, VREF, DO38, 12M A, VREF, DO39, 12M A, VREF, DO40, 12M A, VREF, DO41, 12M A, VREF, DO42, 12M A, VREF, DO43, 12M A, VREF, DO44, 12M A, VREF, DO45, 12M A, VREF, DO46, 12M A, VREF, DO47, 12M A, VREF, DO48, 12M A, VREF, DO49, 12M A, VREF, DO50, 12M A, VREF, DO51, 12M A, VREF, DO52, 12M A, VREF, DO53, 12M A, VREF, DO54, 12M A, VREF, DO55, 12M A, VREF, DO56, 12M A, VREF, DO57, 12M A, VREF, DO58, 12M A, VREF, DO59, 12M A, VREF, DO60, 12M A, VREF, DO61, 12M A, VREF, DO62, 12M A, VREF, DO63, 12M A, VREF, DO64, 12M A, VREF, DO65, 12M A, VREF, DO66, 12M A, VREF, DO67, 12M A, VREF, DO68, 12M A, VREF, DO69, 12M A, VREF, DO70, 12M A, VREF, DO71, 12M A, VREF, DO72, 12M A, VREF, DO73, 12M A, VREF, DO74, 12M A, VREF, DO75, 12M A, VREF, DO76, 12M A, VREF, DO77, 12M A, VREF, DO78, 12M A, VREF, DO79, 12M A, VREF, DO80, 12M A, VREF, DO81, 12M A, VREF, DO82, 12M A, VREF, DO83, 12M A, VREF, DO84, 12M A, VREF, DO85, 12M A, VREF, DO86, 12M A, VREF, DO87, 12M A, VREF, DO88, 12M A, VREF, DO89, 12M A, VREF, DO90, 12M A, VREF, DO91, 12M A, VREF, DO92, 12M A, VREF, DO93, 12M A, VREF, DO94, 12M A, VREF, DO95, 12M A, VREF, DO96, 12M A, VREF, DO97, 12M A, VREF, DO98, 12M A, VREF, DO99, 12M A, VREF, DO100, 12M A, VREF, DO101, 12M A, VREF, DO102, 12M A, VREF, DO103, 12M A, VREF, DO104, 12M A, VREF, DO105, 12M A, VREF, DO106, 12M A, VREF, DO107, 12M A, VREF, DO108, 12M A, VREF, DO109, 12M A, VREF, DO110, 12M A, VREF, DO111, 12M A, VREF, DO112, 12M A, VREF, DO113, 12M A, VREF, DO114, 12M A, VREF, DO115, 12M A, VREF, DO116, 12M A, VREF, DO117, 12M A, VREF, DO118, 12M A, VREF, DO119, 12M A, VREF, DO120, 12M A, VREF, DO121, 12M A, VREF, DO122, 12M A, VREF, DO123, 12M A, VREF, DO124, 12M A, VREF, DO125, 12M A, VREF, DO126, 12M A, VREF, DO127, 12M A, VREF, DO128, 12M A, VREF, DO129, 12M A, VREF, DO130, 12M A, VREF, DO131, 12M A, VREF, DO132, 12M A, VREF, DO133, 12M A, VREF, DO134, 12M A, VREF, DO135, 12M A, VREF, DO136, 12M A, VREF, DO137, 12M A, VREF, DO138, 12M A, VREF, DO139, 12M A, VREF, DO140, 12M A, VREF, DO141, 12M A, VREF, DO142, 12M A, VREF, DO143, 12M A, VREF, DO144, 12M A, VREF, DO145, 12M A, VREF, DO146, 12M A, VREF, DO147, 12M A, VREF, DO148, 12M A, VREF, DO149, 12M A, VREF, DO150, 12M A, VREF, DO151, 12M A, VREF, DO152, 12M A, VREF, DO153, 12M A, VREF, DO154, 12M A, VREF, DO155, 12M A, VREF, DO156, 12M A, VREF, DO157, 12M A, VREF, DO158, 12M A, VREF, DO159, 12M A, VREF, DO160, 12M A, VREF, DO161, 12M A, VREF, DO162, 12M A, VREF, DO163, 12M A, VREF, DO164, 12M A, VREF, DO165, 12M A, VREF, DO166, 12M A, VREF, DO167, 12M A, VREF, DO168, 12M A, VREF, DO169, 12M A, VREF, DO170, 12M A, VREF, DO171, 12M A, VREF, DO172, 12M A, VREF, DO173, 12M A, VREF, DO174, 12M A, VREF, DO175, 12M A, VREF, DO176, 12M A, VREF, DO177, 12M A, VREF, DO178, 12M A, VREF, DO179, 12M A, VREF, DO180, 12M A, VREF, DO181, 12M A, VREF, DO182, 12M A, VREF, DO183, 12M A, VREF, DO184, 12M A, VREF, DO185, 12M A, VREF, DO186, 12M A, VREF, DO187, 12M A, VREF, DO188, 12M A, VREF, DO189, 12M A, VREF, DO190, 12M A, VREF, DO191, 12M A, VREF, DO192, 12M A, VREF, DO193, 12M A, VREF, DO194, 12M A, VREF, DO195, 12M A, VREF, DO196, 12M A, VREF, DO197, 12M A, VREF, DO198, 12M A, VREF, DO199, 12M A, VREF, DO200, 12M A, VREF, DO201, 12M A, VREF, DO202, 12M A, VREF, DO203, 12M A, VREF, DO204, 12M A, VREF, DO205, 12M A, VREF, DO206, 12M A, VREF, DO207, 12M A, VREF, DO208, 12M A, VREF, DO209, 12M A, VREF, DO210, 12M A, VREF, DO211, 12M A, VREF, DO212, 12M A, VREF, DO213, 12M A, VREF, DO214, 12M A, VREF, DO215, 12M A, VREF, DO216, 12M A, VREF, DO217, 12M A, VREF, DO218, 12M A, VREF, DO219, 12M A, VREF, DO220, 12M A, VREF, DO221, 12M A, VREF, DO222, 12M A, VREF, DO223, 12M A, VREF, DO224, 12M A, VREF, DO225, 12M A, VREF, DO226, 12M A, VREF, DO227, 12M A, VREF, DO228, 12M A, VREF, DO229, 12M A, VREF, DO230, 12M A, VREF, DO231, 12M A, VREF, DO232, 12M A, VREF, DO233, 12M A, VREF, DO234, 12M A, VREF, DO235, 12M A, VREF, DO236, 12M A, VREF, DO237, 12M A, VREF, DO238, 12M A, VREF, DO239, 12M A, VREF, DO240, 12M A, VREF, DO241, 12M A, VREF, DO242, 12M A, VREF, DO243, 12M A, VREF, DO244, 12M A, VREF, DO245, 12M A, VREF, DO246, 12M A, VREF, DO247, 12M A, VREF, DO248, 12M A, VREF, DO249, 12M A, VREF, DO250, 12M A, VREF, DO251, 12M A, VREF, DO252, 12M A, VREF, DO253, 12M A, VREF, DO254, 12M A, VREF, DO255, 12M A, VREF, DO256, 12M A, VREF, DO257, 12M A, VREF, DO258, 12M A, VREF, DO259, 12M A, VREF, DO260, 12M A, VREF, DO261, 12M A, VREF, DO262, 12M A, VREF, DO263, 12M A, VREF, DO264, 12M A, VREF, DO265, 12M A, VREF, DO266, 12M A, VREF, DO267, 12M A, VREF, DO268, 12M A, VREF, DO269, 12M A, VREF, DO270, 12M A, VREF, DO271, 12M A, VREF, DO272, 12M A, VREF, DO273, 12M A, VREF, DO274, 12M A, VREF, DO275, 12M A, VREF, DO276, 12M A, VREF, DO277, 12M A, VREF, DO278, 12M A, VREF, DO279, 12M A, VREF, DO280,



Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)



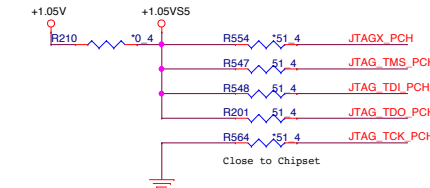
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit				
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode					
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)					
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC0 				
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden	34 GPIO33_EC 				
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC SPI(Default)</td></tr></tbody></table>	GNT0#	Boot Location	1	LPC SPI(Default)	
GNT0#	Boot Location							
1	LPC SPI(Default)							
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality					
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC0 				
				<div>34 PCH_SPI_CS0#_RPCH_SPI_CS0#_R</div> <div>34 PCH_SPI1_CLK_RPCH_SPI1_CLK_R</div> <div>34 PCH_SPI1_SI_RPCH_SPI1_SI_R</div> <div>34 PCH_SPI1_SO_RPCH_SPI1_SO_R</div>				

HDD (SATA3 6.0Gb/s)

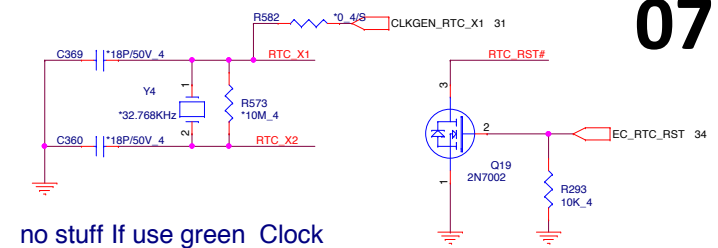
ODD (SATA2 3.0Gb/s)

mSATA / NGFF (SATA4 6Gb/s)



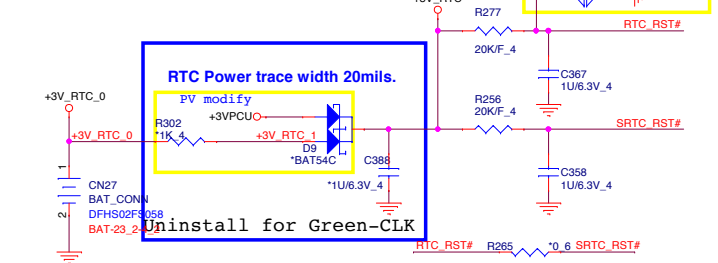
DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

RTC Clock 32.768KHz

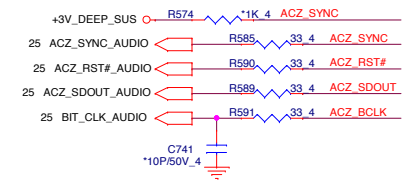


no stuff if use green Clock

RTC Circuitry(RTC)



HDA Bus(CLG)

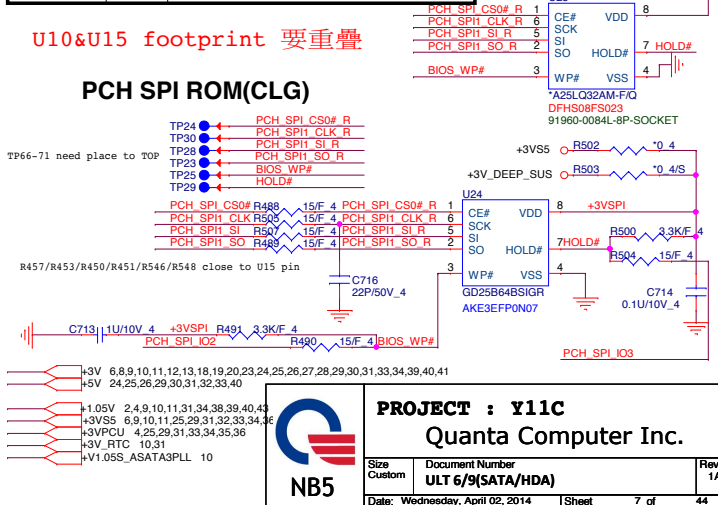


GPIO Pull UP

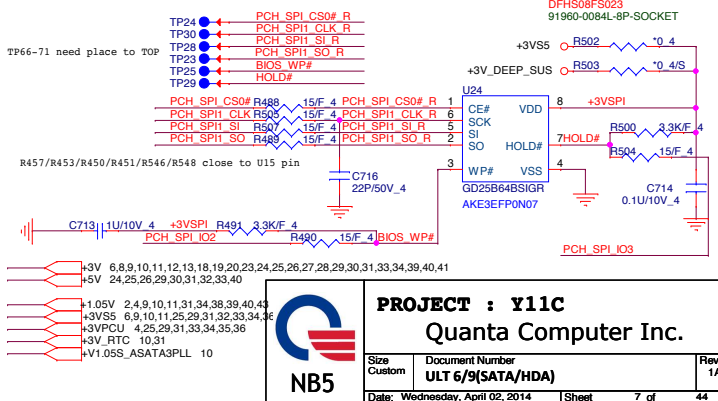


Vender	Size	P/N
MXIC	8MB	AKE3EZN0Z00 (MX25L6473EM2I-10G)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket



PCH SPI ROM(CLG)

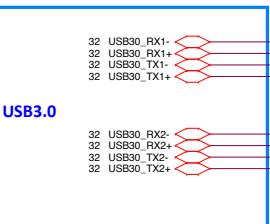
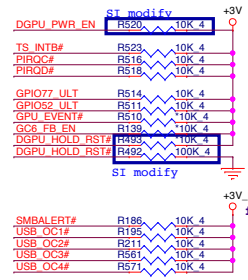


PROJECT : Y11C
Quanta Computer Inc.

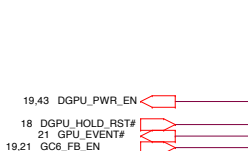
Size Custom	Document Number ULT 6/9(SATA/HDA)	Rev 1A
Date: Wednesday, April 02, 2014	Sheet 7 of	44

Lynx Point-LP Platform Controller Hub
(HDA, JTAG, SATA)

PCI/USBOC# Pull-up(CLG)



20111130 Modify USB3.0 for HM70



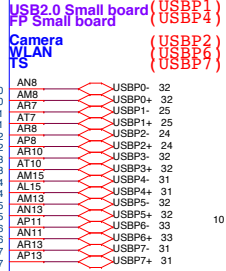
Cardreader

WLAN

LAN

C-Link

USB2.0(WB-1) (USBP0)
USB2.0(WB-2) (USBP1)
USB2.0 Small board (USBP4)
FP Small board (USBP5)
Camera (USBP6)
WLAN (USBP7)

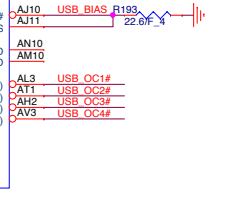


Cardreader

WLAN

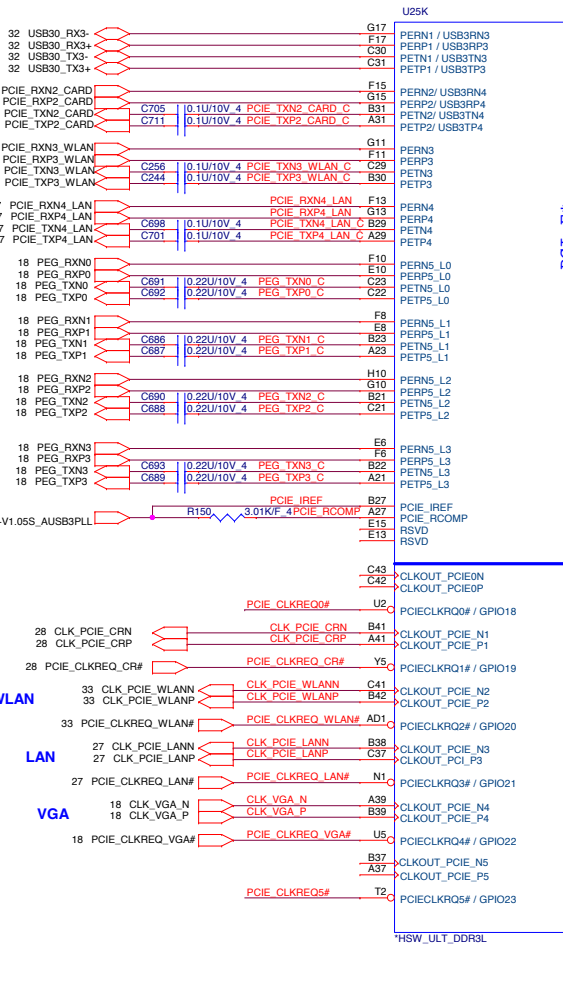
LAN

VGA



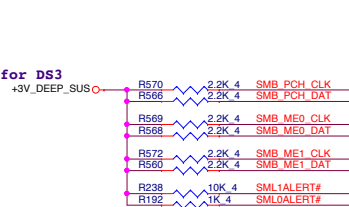
PCI-E*

CLOCK SIGNALS



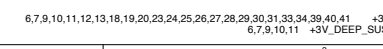
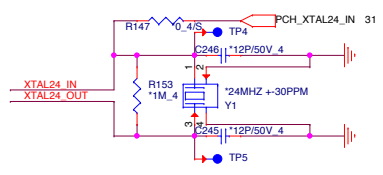
SMBUS

SMBus/Pull-up(CLG)

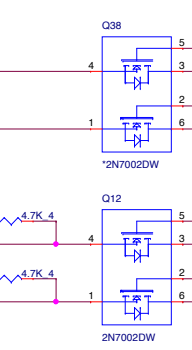


PROJECT : Y11C
Quanta Computer Inc.

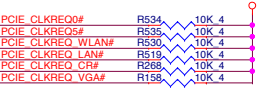
Size Custom	Document Number	Rev 1A
ULT 7/9 (PCIe/USB/CLK)		
Date: Wednesday, April 02, 2014	Sheet	8 of 44



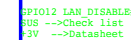
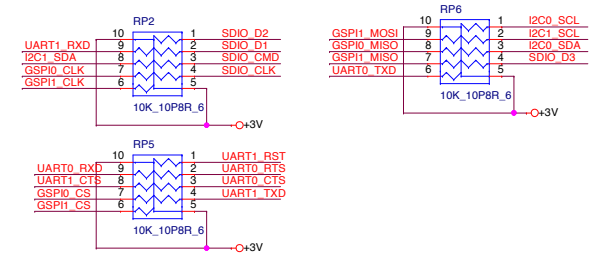
SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)

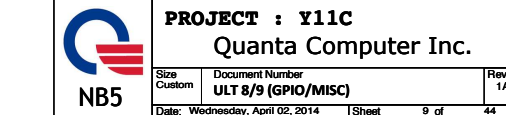


09

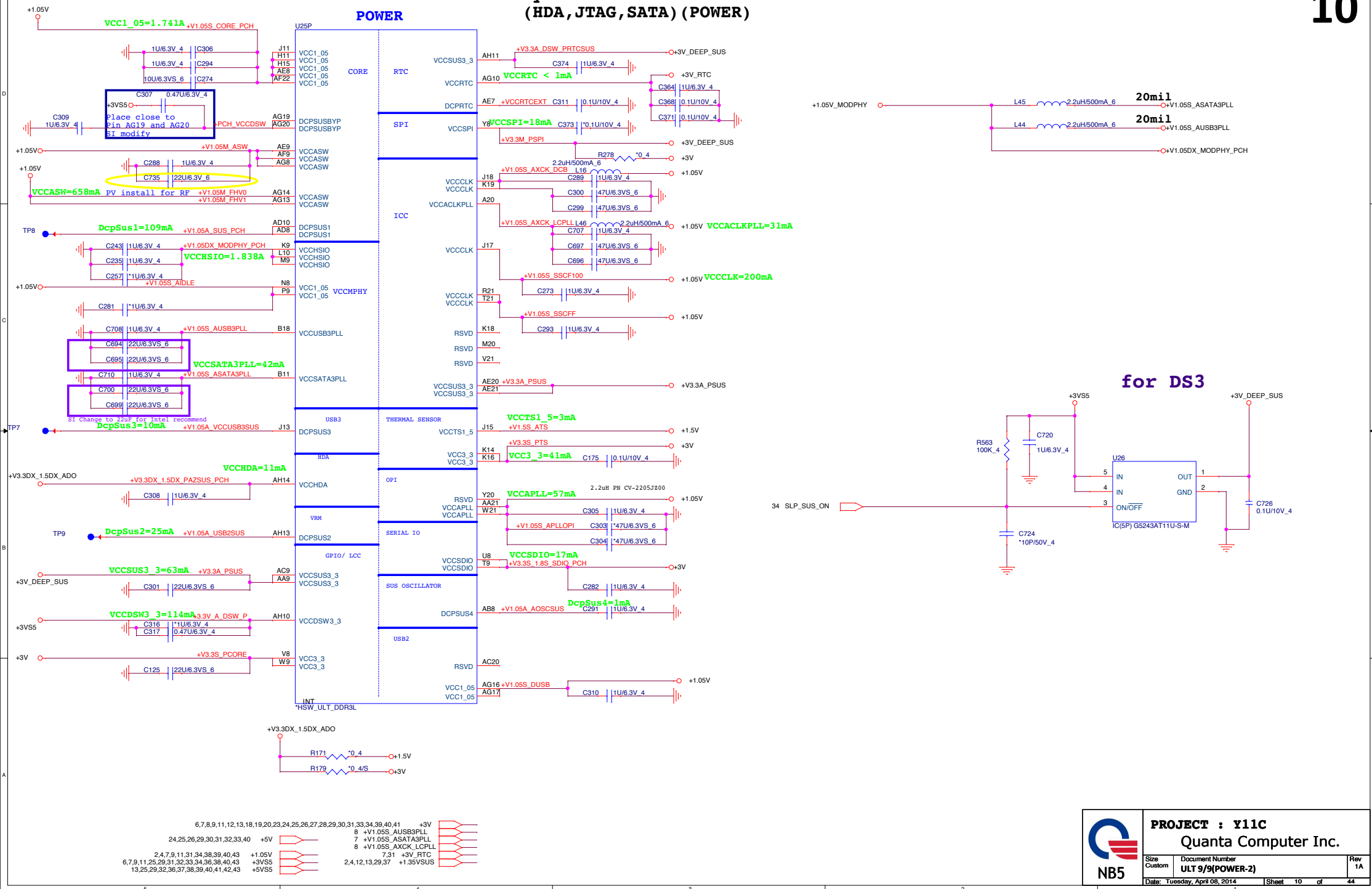


The schematic diagram illustrates a 10-bit DAC using a resistor ladder network. The network is composed of 10 resistors, labeled R174 through R183, arranged in a ladder configuration. The top of the ladder is connected to a 3V_DEEP_SUS supply, and the bottom is connected to ground. The output of the DAC is taken from the node between R174 and R175. The resistors are labeled with their values (10K 4) and the board IDs (BOARD_ID0 to BOARD_ID9).

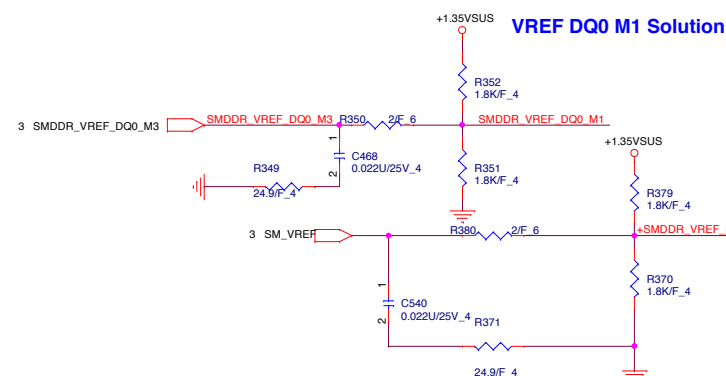
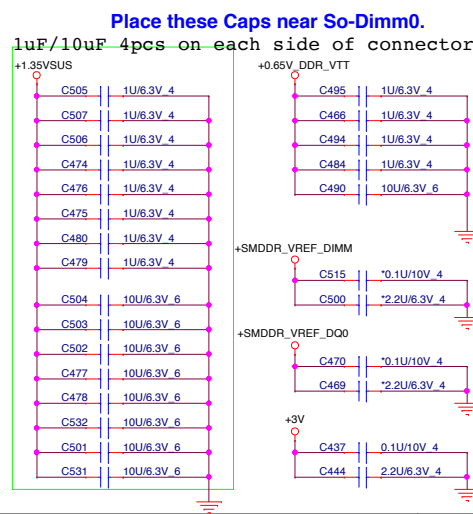
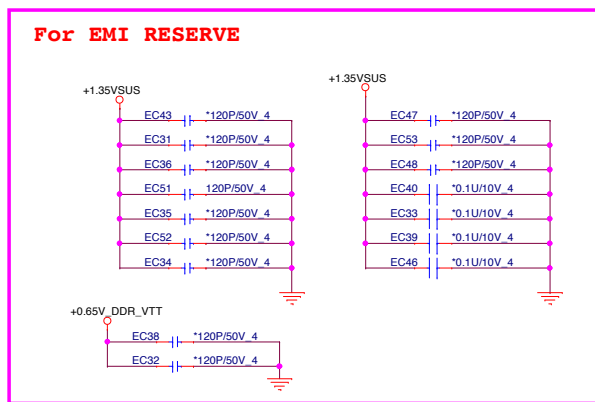
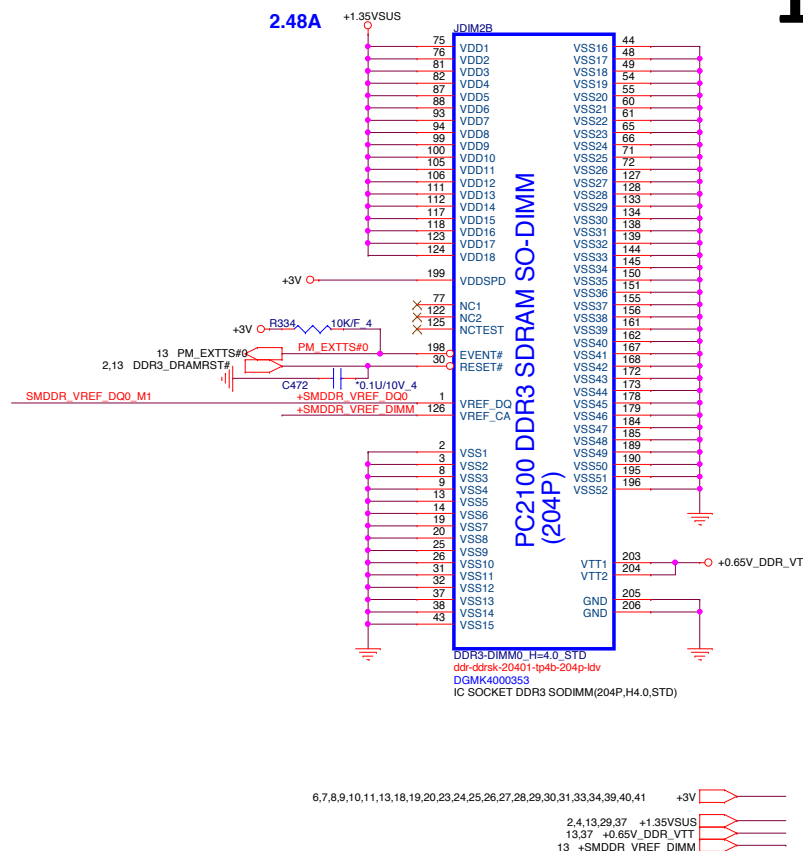
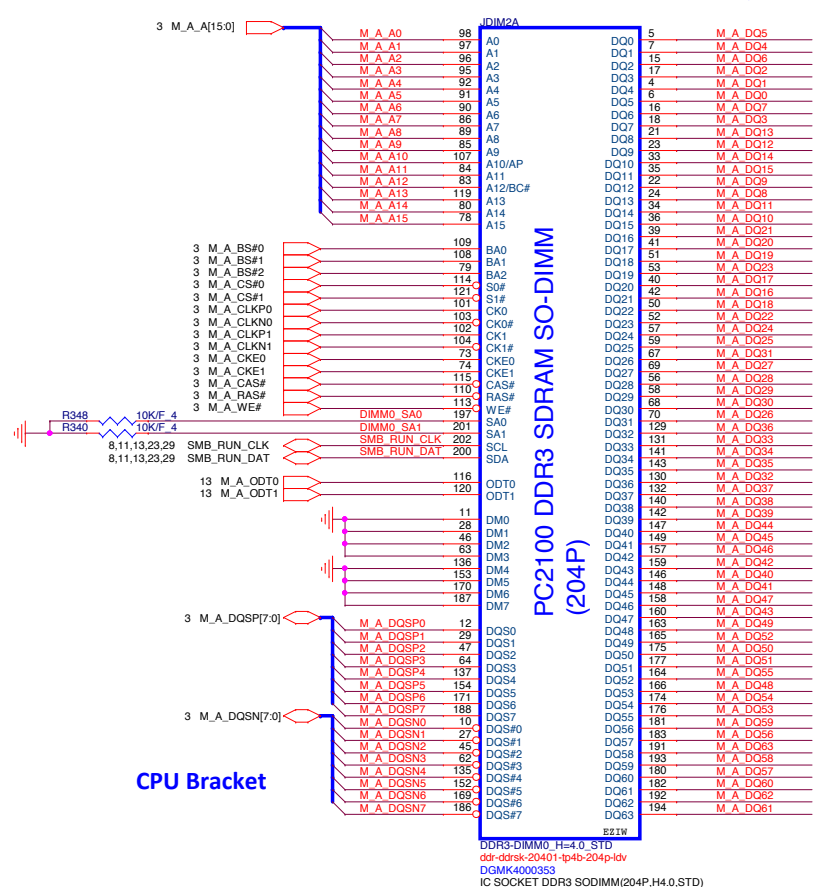
6,7,8,10,11,12,13,18,19,20,23,24,25,26,27,28,29,30,31,33,34,39,40,41 +3V
6,7,10,11,25,29,31,32,33,34,36,38,40,43 +3VS5



Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA) (POWER)

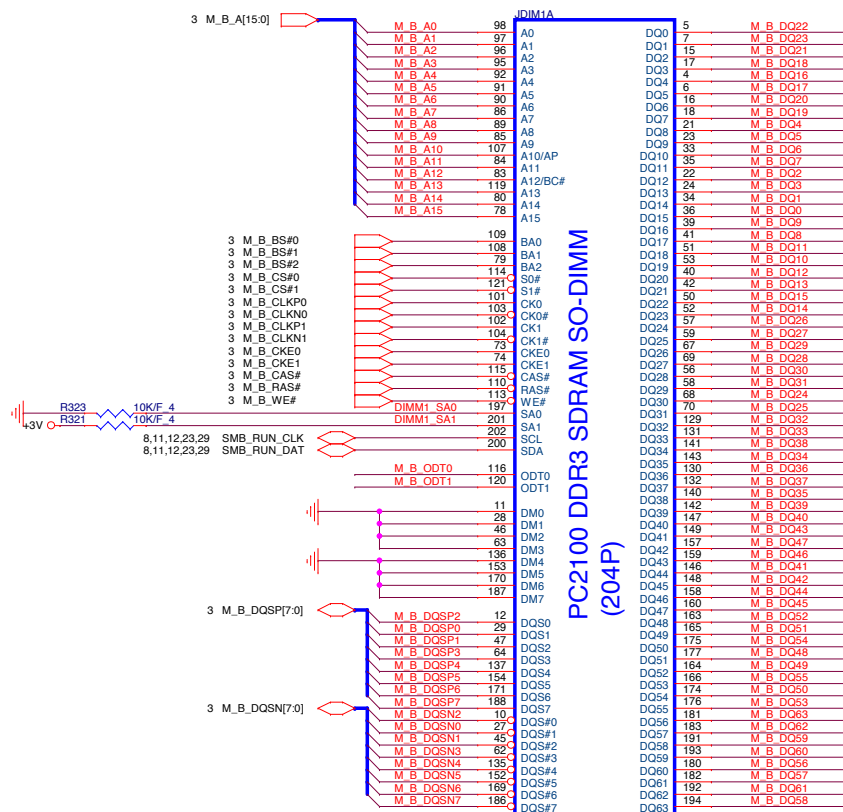









DIMM & Footprint 同Joshua提供

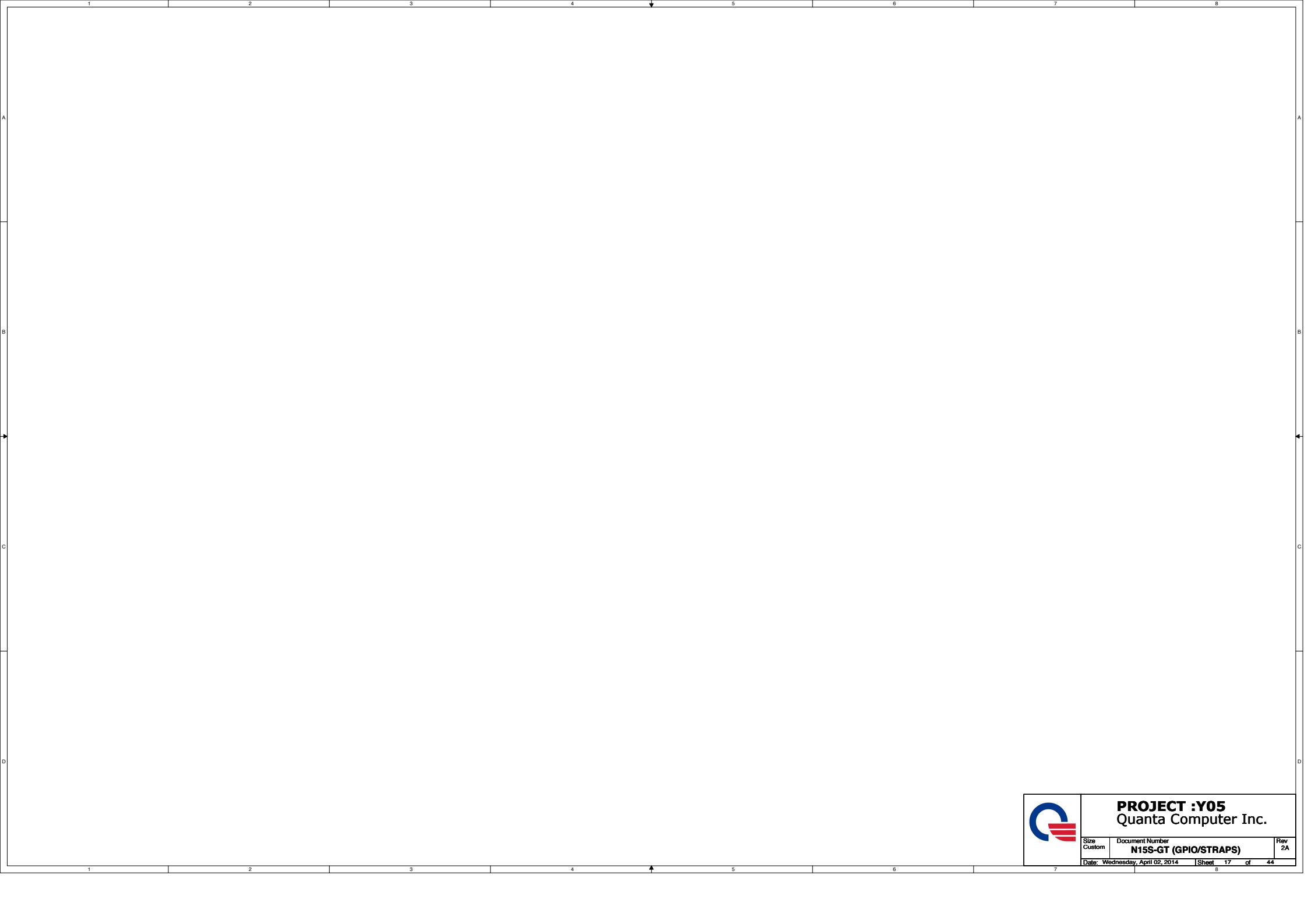
M_B_DQ[63:0] 3



	PROJECT :Y05 Quanta Computer Inc.		
	Size Custom	Document Number N15S-GT (PCIe VF) /NVDD	Rev 2A
	Date: Wednesday, April 02, 2014 Sheet 14 of 44		

	PROJECT :Y05 Quanta Computer Inc.		
	Size Custom	Document Number N15S-GT (MEMORY/GND)	Rev 2A
	Date: Wednesday, April 02, 2014		Sheet 15 of 44

	PROJECT :Y05 Quanta Computer Inc.		
	Size Custom	Document Number N15S-GT (DISPLAY)	Rev 2A
	Date: Wednesday, April 02, 2014		Sheet 16 of 44




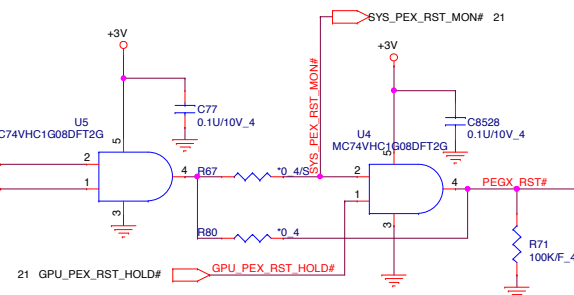
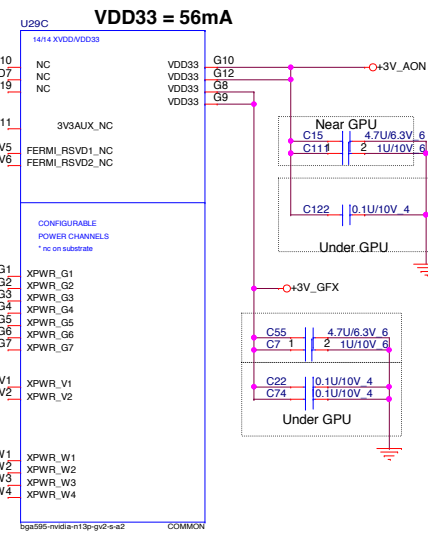
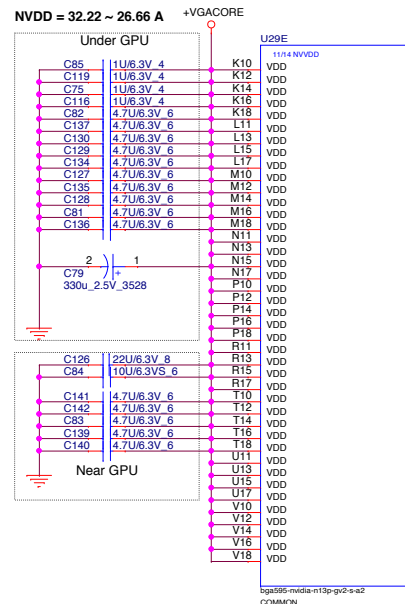
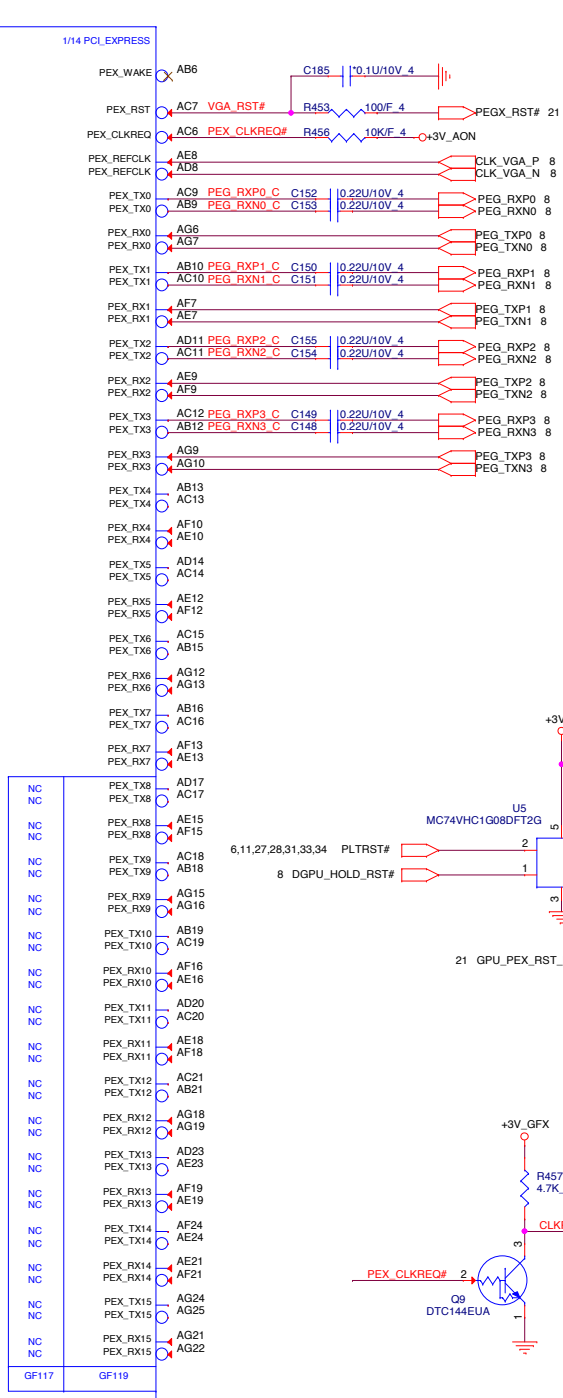
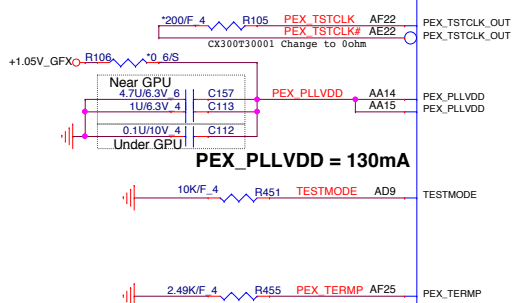
	PROJECT :Y05 Quanta Computer Inc.		
	Size Custom	Document Number N15S-GT (GPIO/STRAPS)	Rev 2A
	Date: Wednesday, April 02, 2014		Sheet 17 of 44

Figure 10 shows the pin connections for the PEX_10VDDX and PEX_10VDDY power planes. The diagram is divided into two main sections: 'Near GPU' and 'Under GPU'. Each section lists pins and their corresponding voltage and current specifications.

Section	Pin	Voltage	Current	Notes
Near GPU	C191	1.05V_8V_6	6	A110
	C186	1.02V_8V_6	6	A112
	C195	1.01V_8V_6	6	A113
	C187	1.00V_8V_6	6	A116
	C189	4.70V_3V_6	6	A118
				A119
				A120
				A121
				A122
				A123
Under GPU	C147	1.01V_3V_4	4	A254
	C144	1.01V_10V_4	4	A255
				A256
				A257
				A258
				A259
				A260
				A261
				A262
				A263

The schematic diagram shows the PLL and SVDD circuit. It features a +3V_{AON} input and a ground connection. A dashed box labeled "Near GPU" contains three capacitors: C56 (10.1U/10V 4), C16 (4.7U/6.3V 6), and C14 (4.7U/6.3V 6). The circuit is connected to output pins AA8, AA9, and AB8. AA8 and AA9 are labeled PEX_PLL_HV1 and PEX_PLL_HV2 respectively. AB8 is labeled PEX_SVDD_3.



VDD33
+3.3V_GFX

NVDD
+VCC_DGFX_CORE

FBVDDQ
+1.5V_GFX

PEX_VDD
+1.05V_GFX

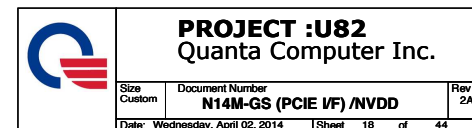
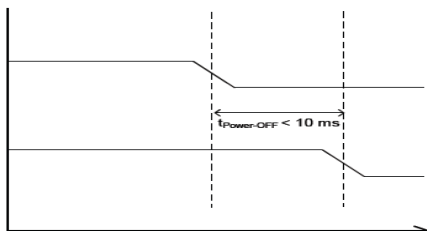
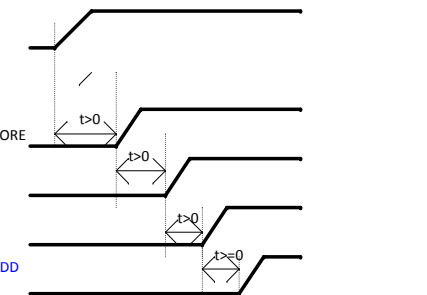
IFP(CDEF)_IOVDD
+1.05V_GFX

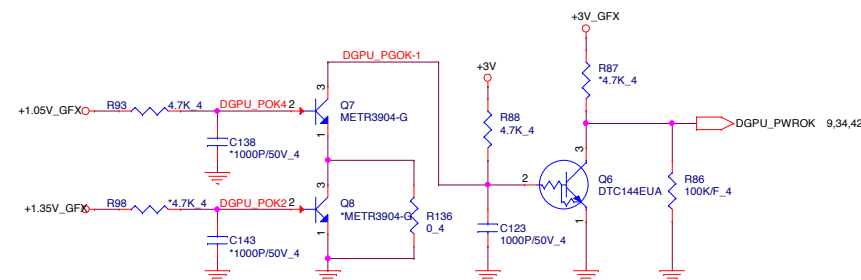
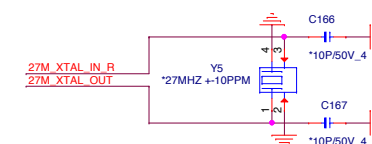
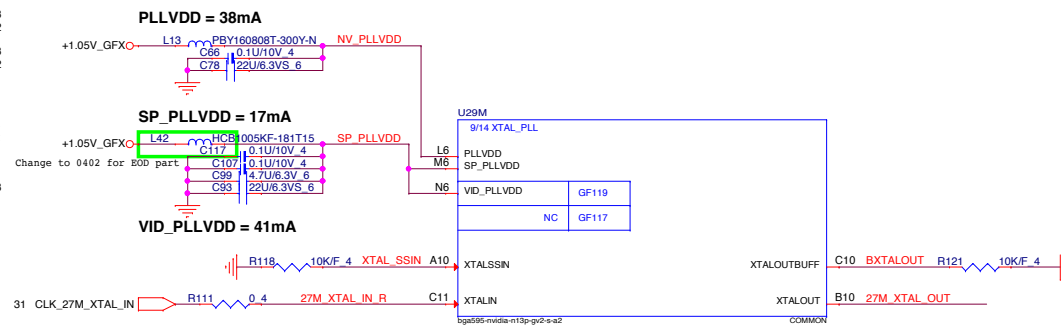
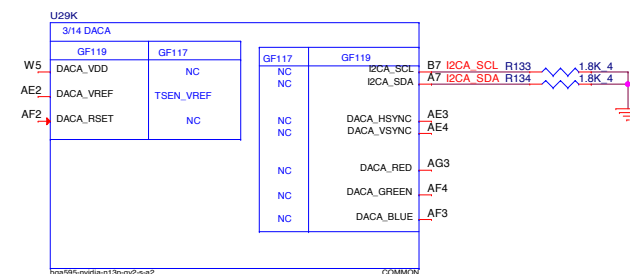
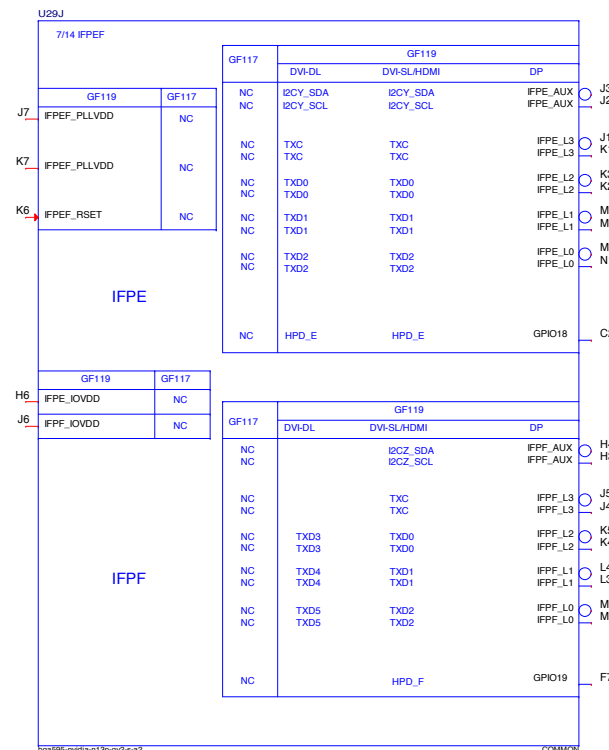
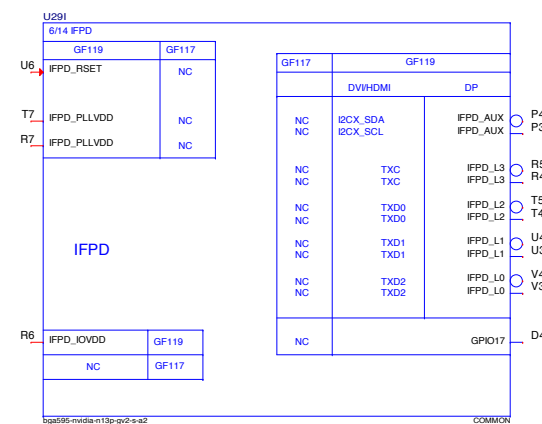
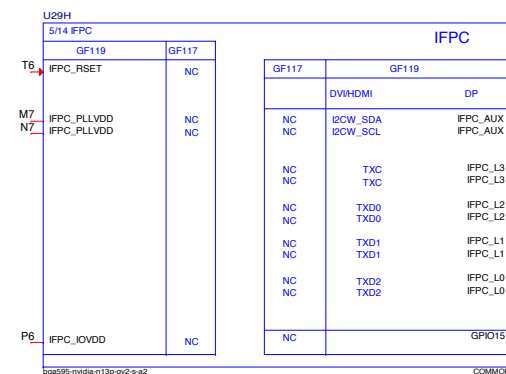
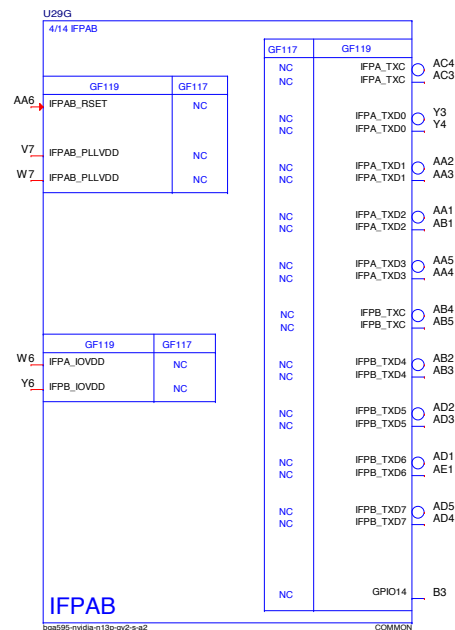
First Rail to Power

First Rail to Power

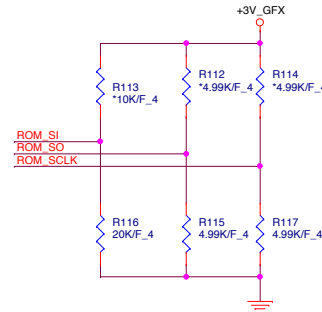
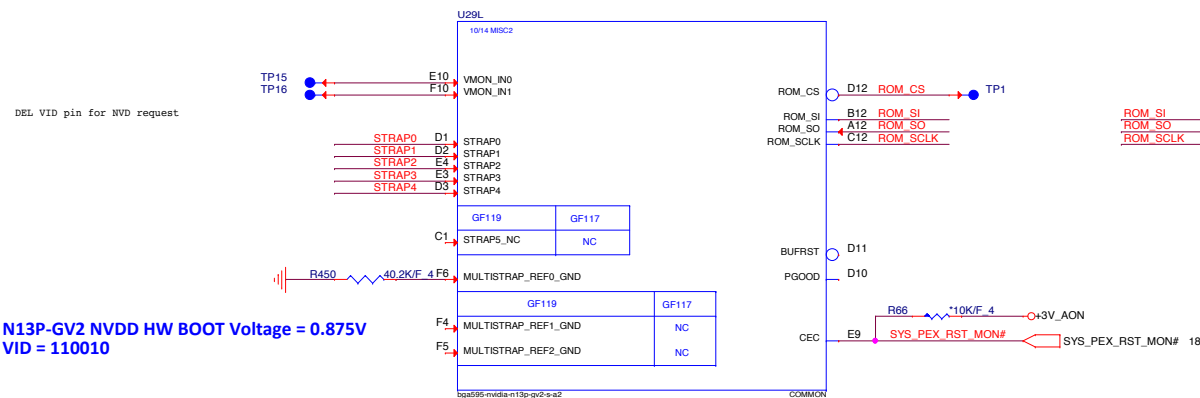
Last Rail to
Power
Down

Last Rail to
Power
Down





N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010



Default: HYNIX

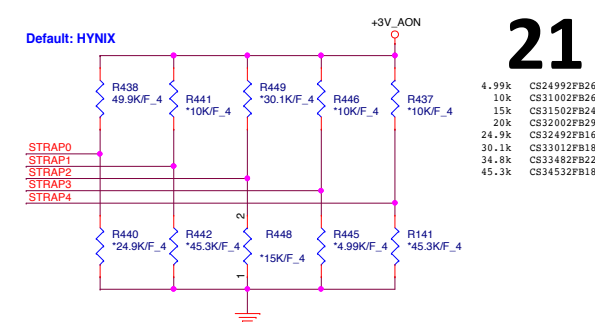
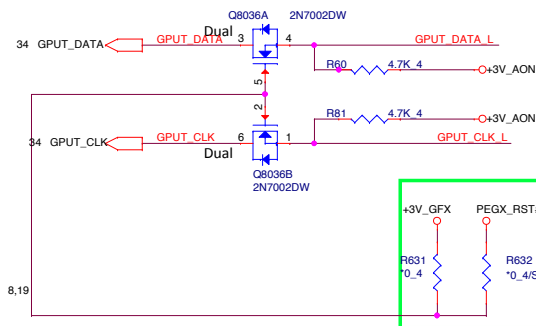
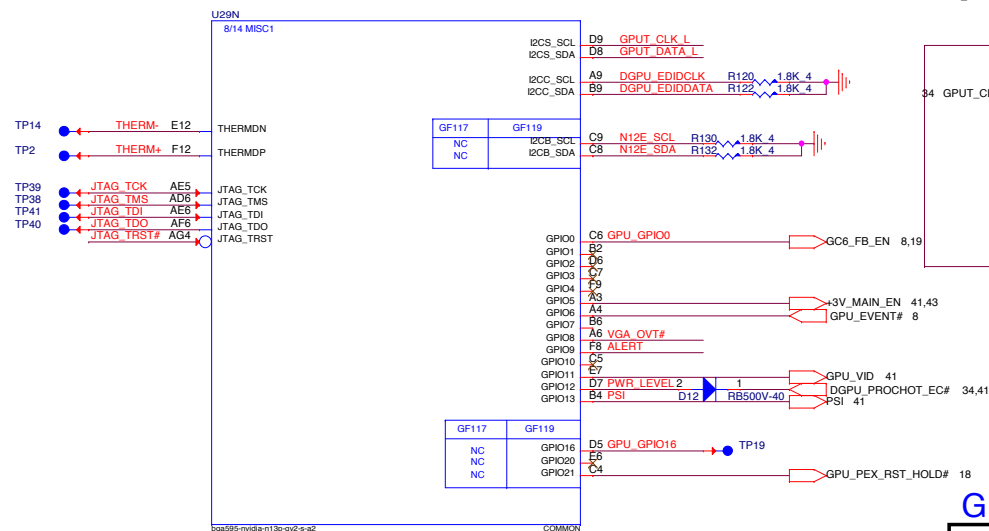


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Hynix should be 0x3, R440 20K 1%
Micro Should be 0x4, R440 24.9K 1%
Samsung Should be 0x5, R440 30.1K 1%

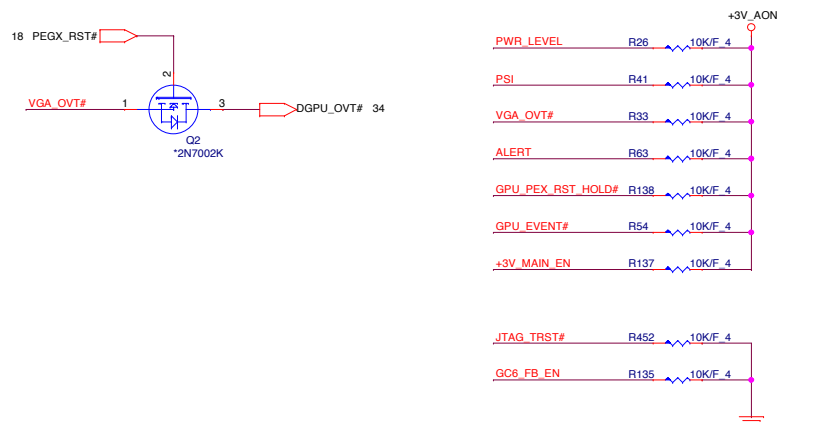


VRAM Configuration Table ROM_SI

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	QBC	TOP B/S
0000	DDR3 256Mx16, 64bit, 4Gb,900MHz	...	MT41J256M16HA-093G:E	S-M	AKD5PZSTL01	AKD5PZSTL00
0100	DDR3 256Mx16, 64bit, 4Gb,900MHz	Micron	H5TC4G63AFR-11C	AKD5PGWT500	AKD5PGWTW08	AKD5PGWTW07
0011	DDR3 256Mx16, 64bit, 4Gb,900MHz	HYNIX	4W4G1646D-BC1A			
0101		SAMSUNG				

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



PROJECT :U82
Quanta Computer Inc.

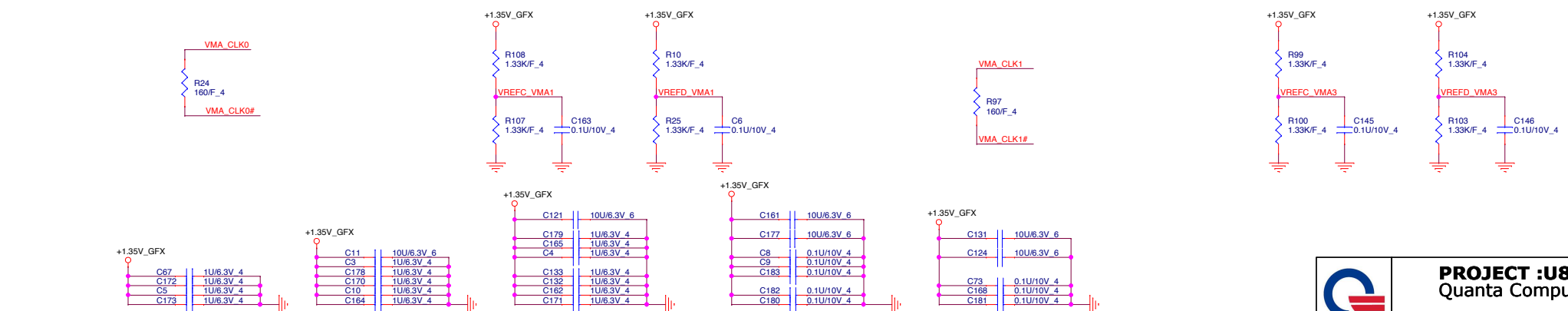
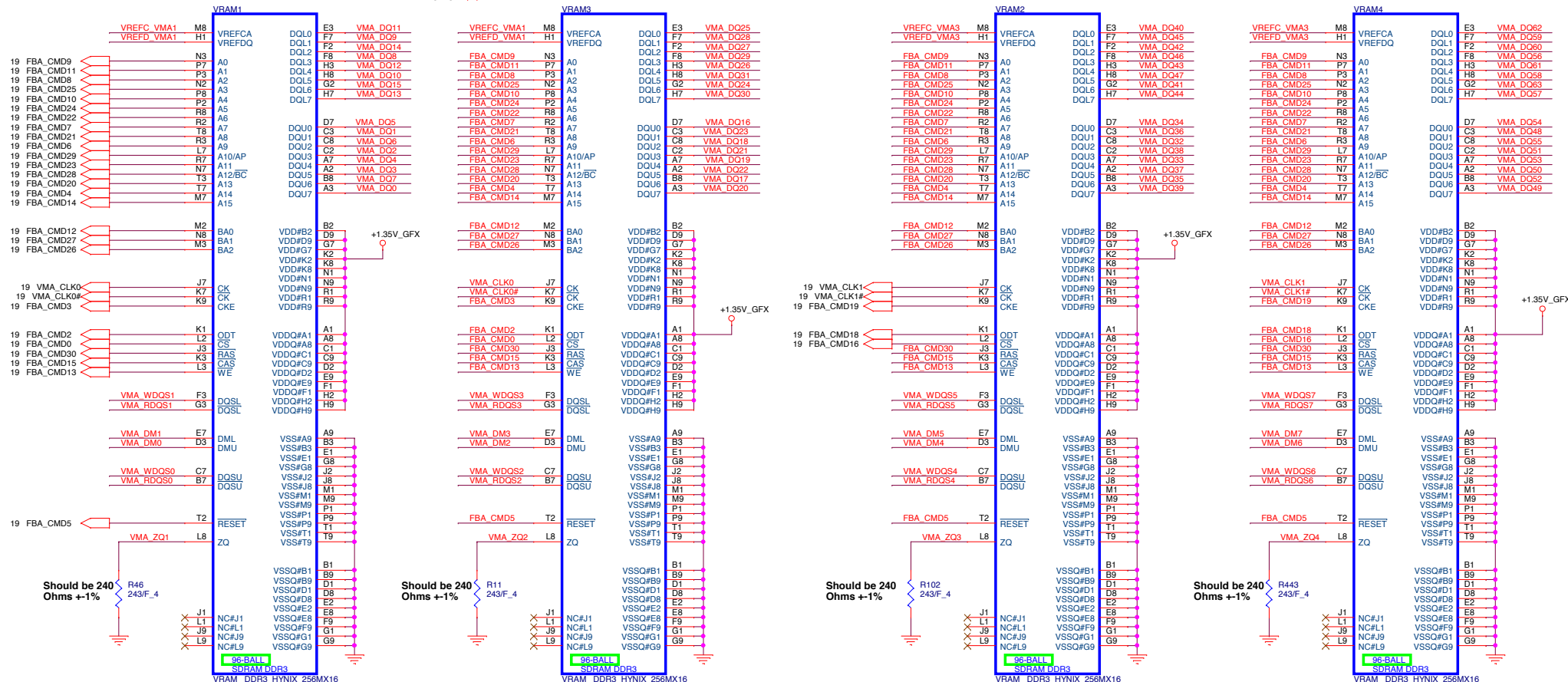
Size Custom	Document Number	Rev
	N14M-GS (GPIO/STRAPS)	2A
Date: Tuesday, April 08, 2014	Sheet 21 of 44	

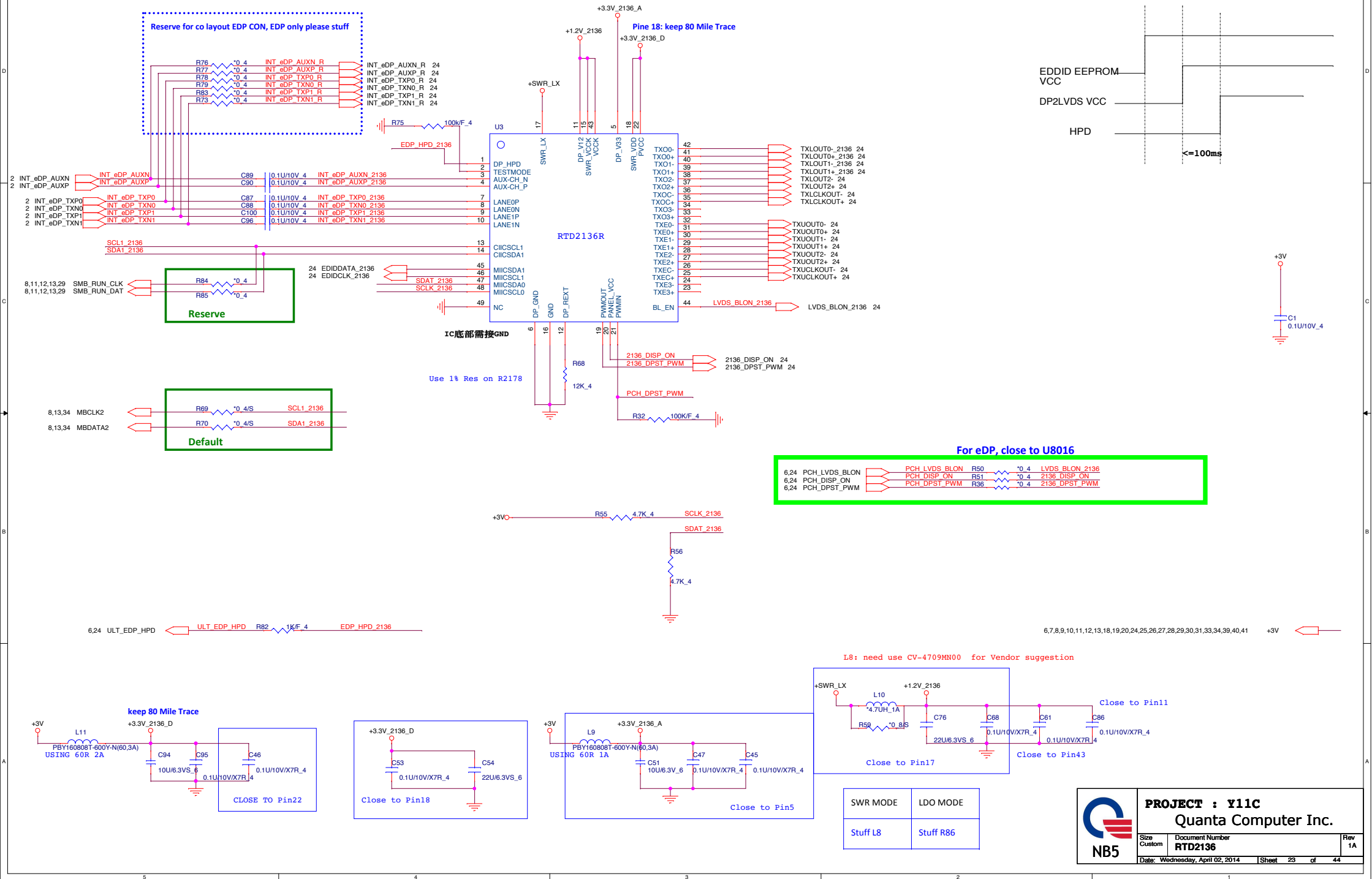
CHANNEL A: 256MB/512MB DDR3

22

HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02
SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534

19 VMA_DQ[63..0]
19 VMA_DM[7..0]
19 VMA_WDQS[7..0]
19 VMA_RDQS[7..0]

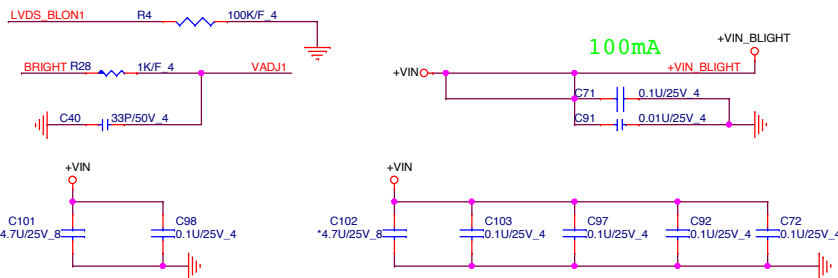
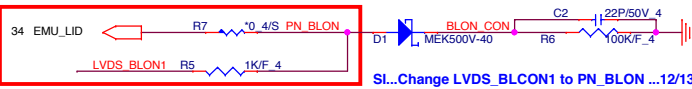




LID Switch

LVDS Conn.

24



For LVDS Power Switch Reserve 80 mile trace

SI...Change R23 Netname to "DISP_ON" ...11/30
SI...ADD R139for LVDS DISO ON ...11/30

for eDP

R31 close to U2 for eDP,stuff

AP2821KTR-G1

for eDP,stuff U2 & L8

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

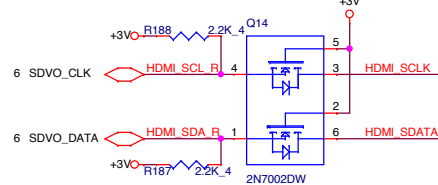
for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

for LVDS,stuff C29 & R23

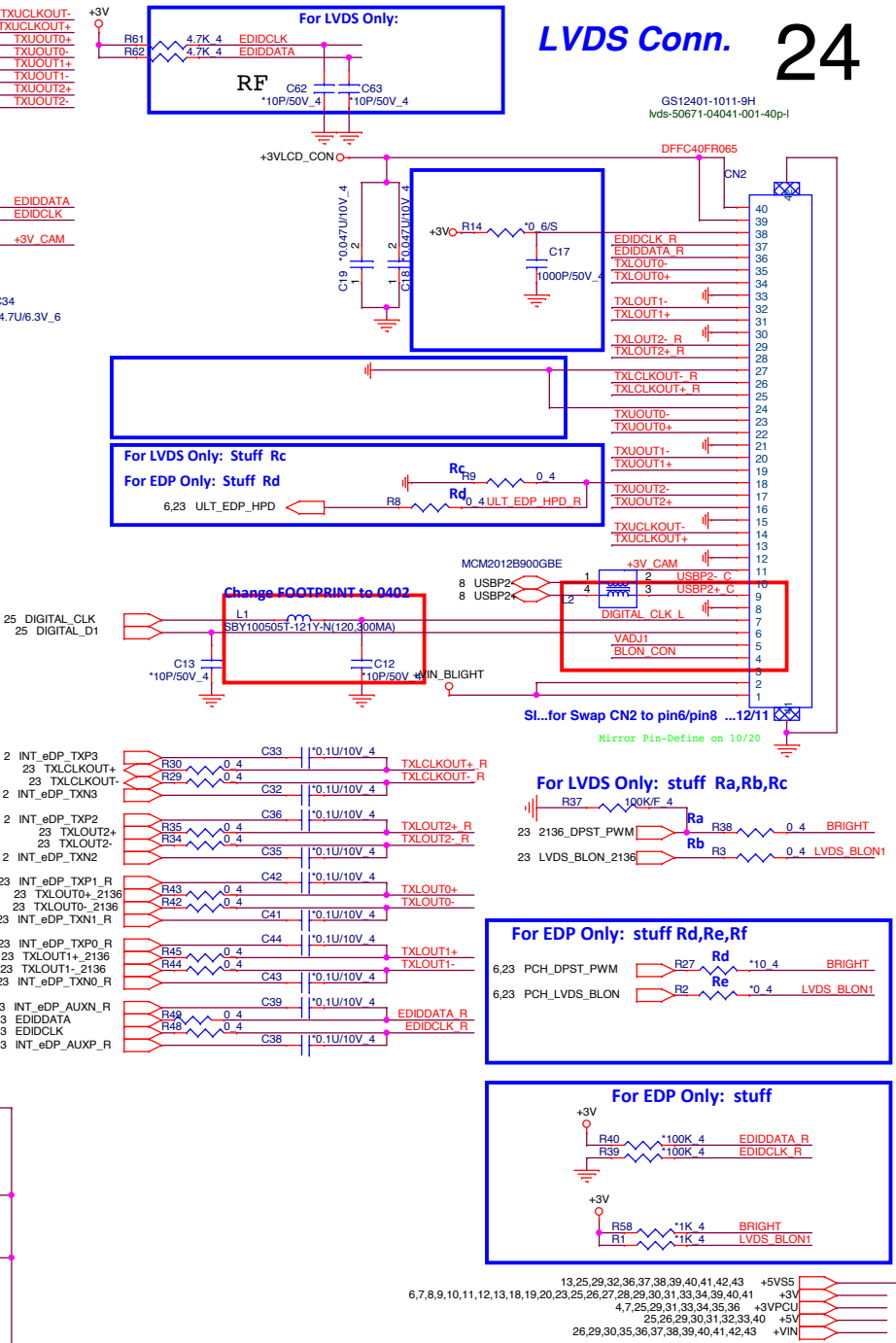
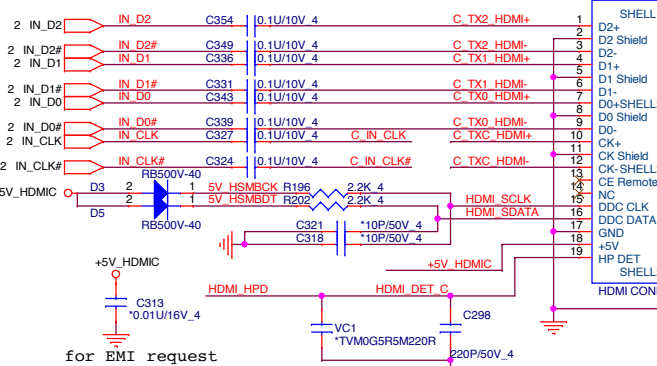
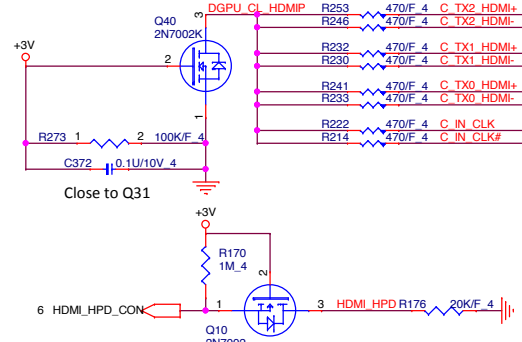
for LVDS,stuff C29 & R23

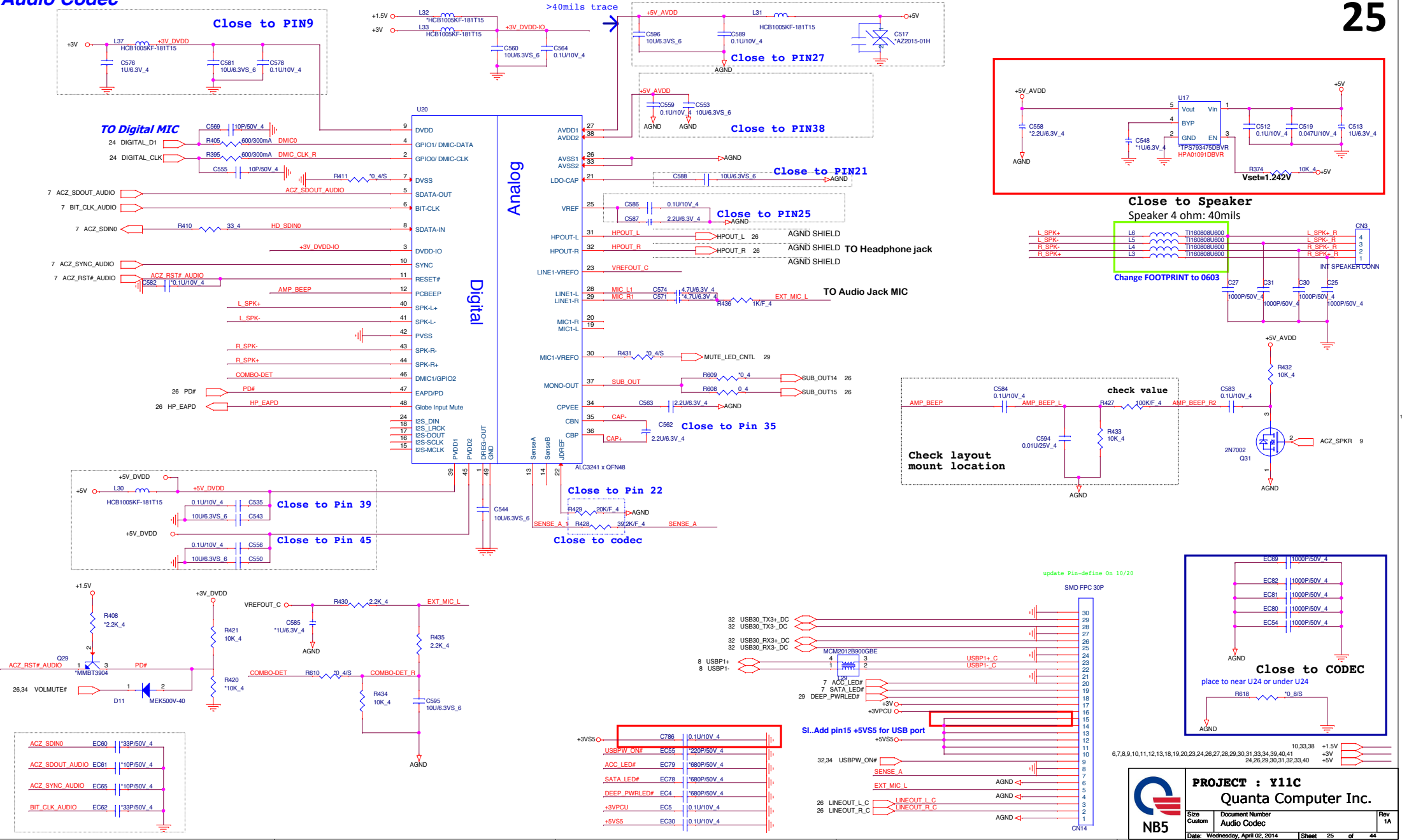
HDMI SMBus Isolation

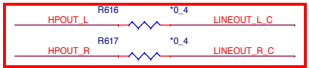


For EDP Only: stuff Cap
For LVDS only stuff Resistor

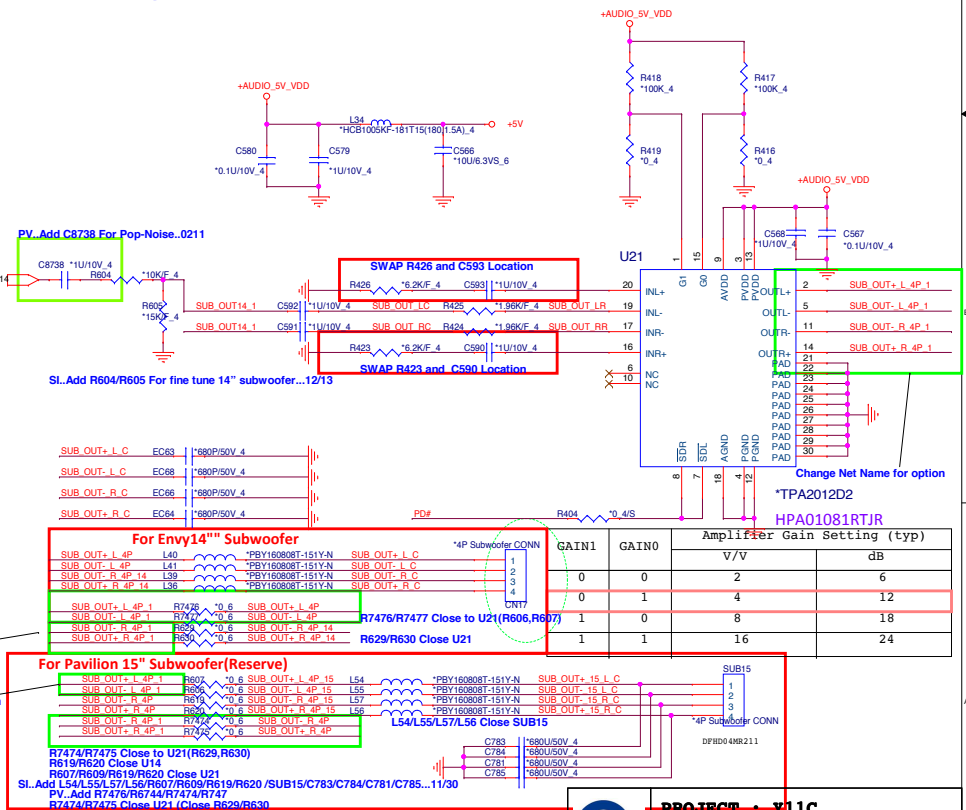
Close to HDMI connector







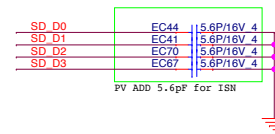
***For Pavilion 15" Subwoofer(Reserve)
For Envy14"" Subwoofer***



GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36



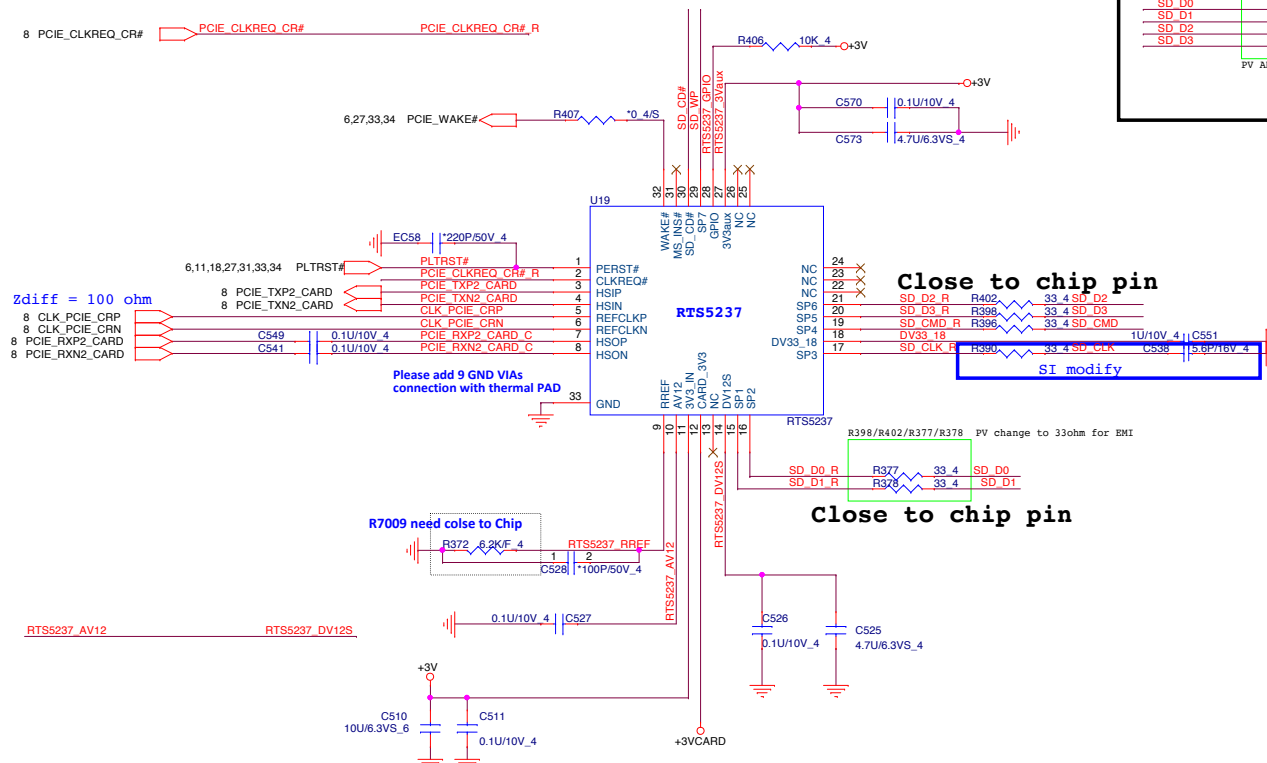
Reserve for EMI



SP1	SD D1	
SP2	SD D0	MS D0
SP3	SD CLK	MS D1
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin

SD / MMC

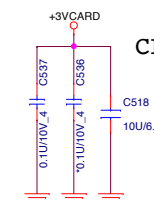


Close to chip pin

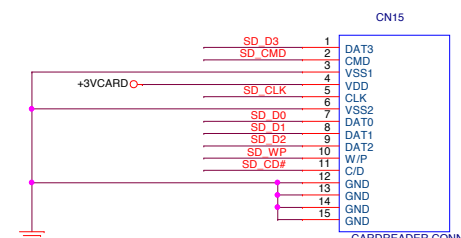
SI modify

Close to chip pin

CLOSE CONN

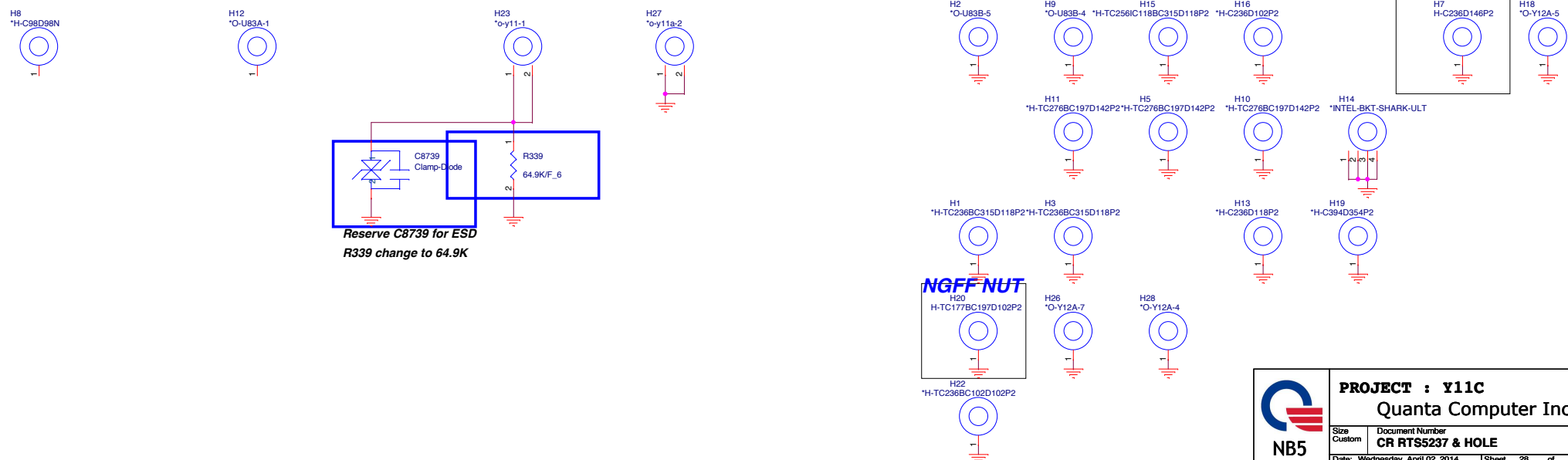


CARD READER



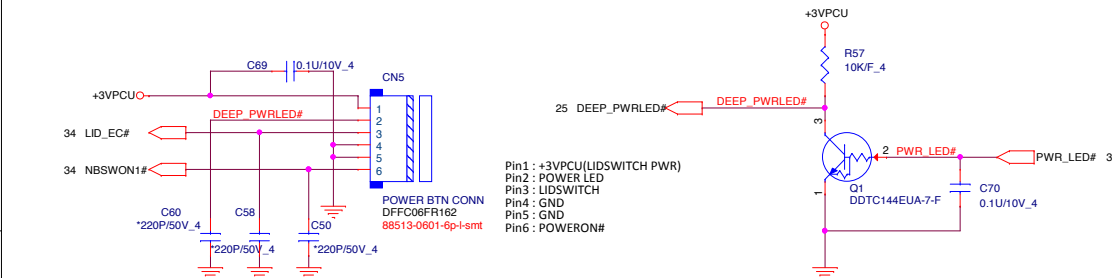
R6x Type

Thermal Nut

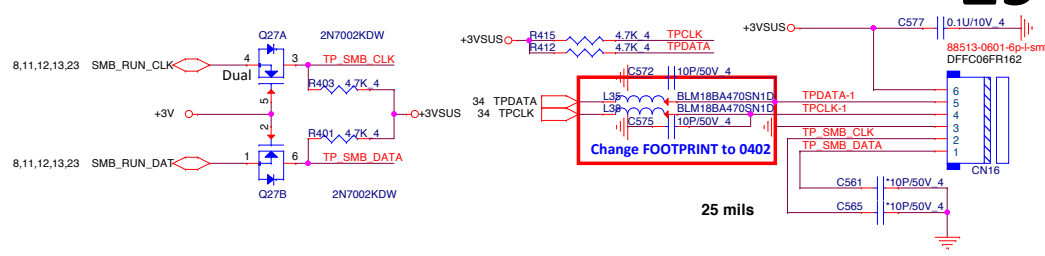


Reserve C8739 for ESD
R339 change to 64.9K

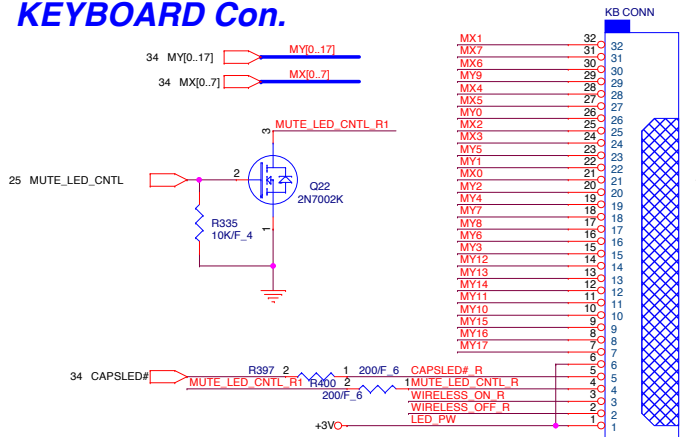
NGFF NUT



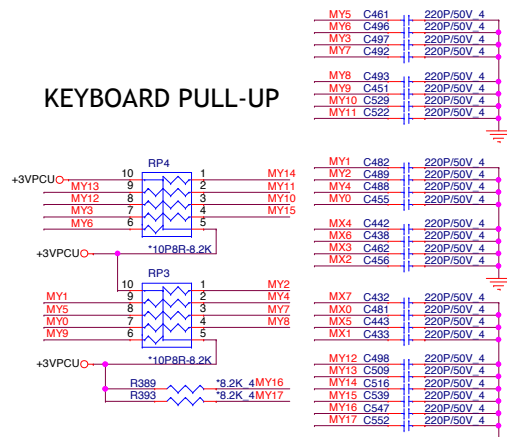
Touch Pad Connector



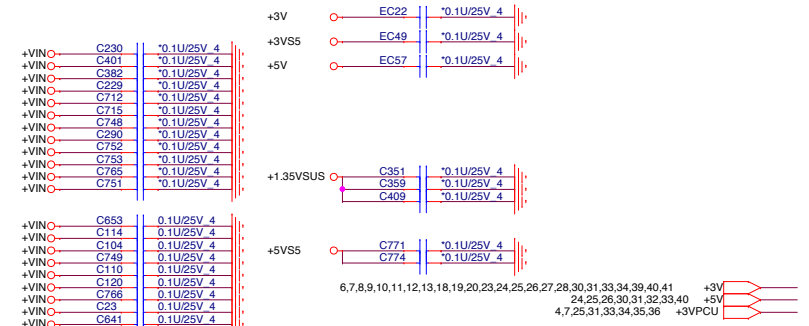
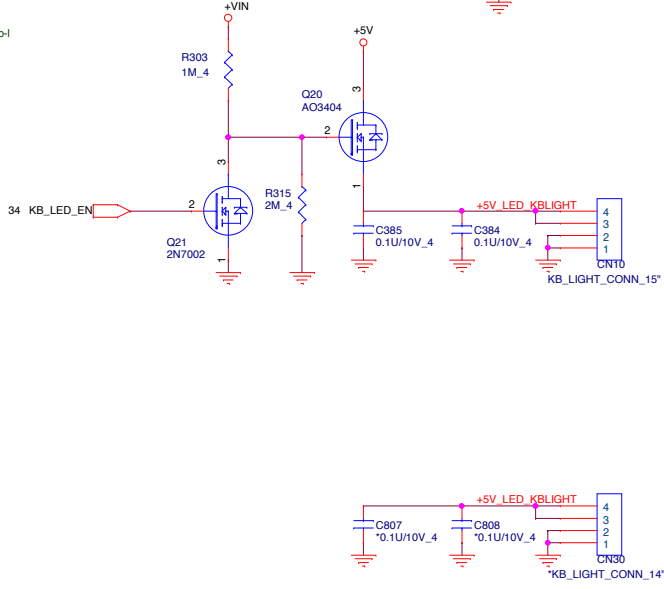
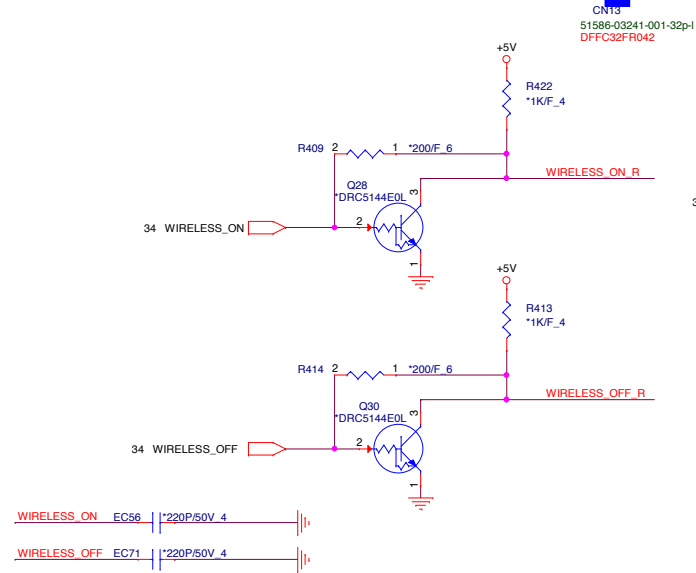
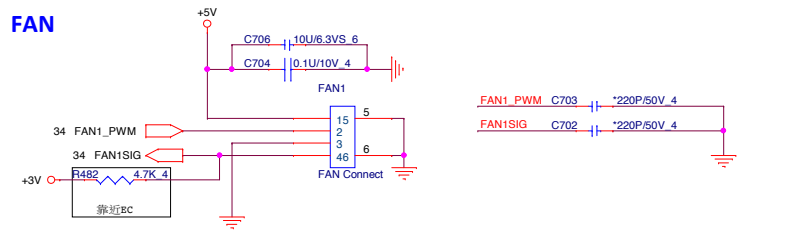
KEYBOARD Con.



KEYBOARD PULL-UP

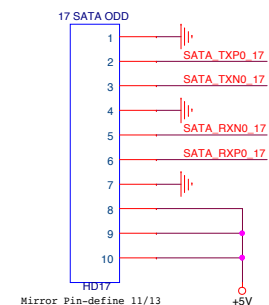
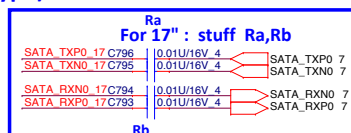


FAN

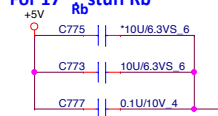


HDD

SATA HDD Connector(Cable type) 15.6"

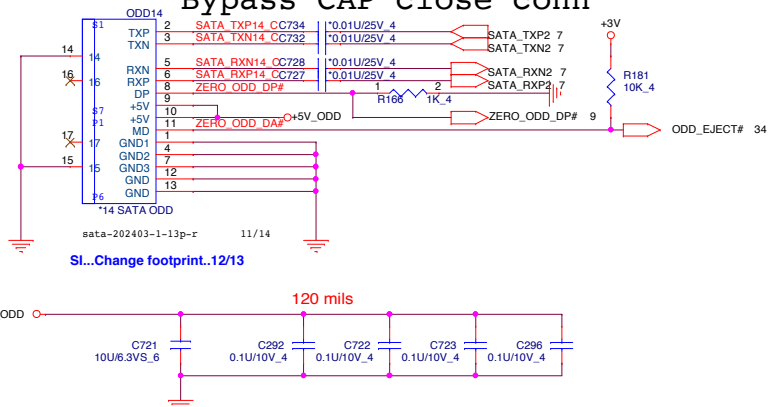


For 17" : stuff Rb

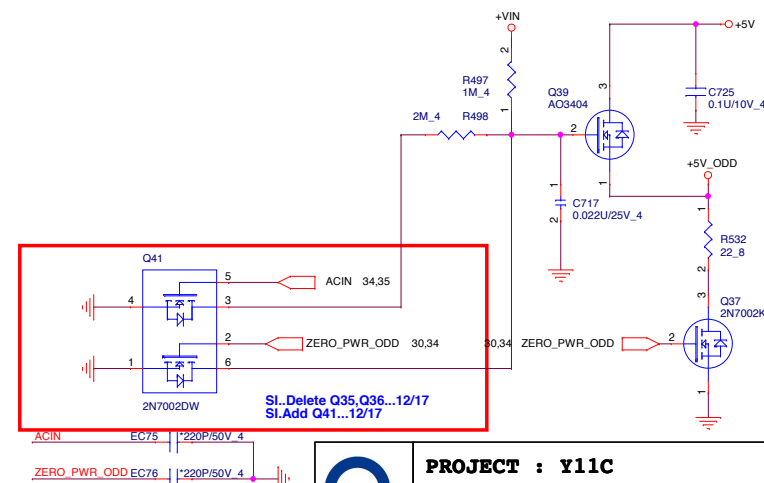
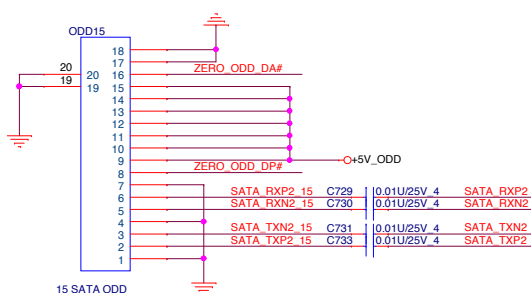
SATA ODD
CONNECTOR

14" SATA ODD

Bypass CAP close conn



15" SATA ODD



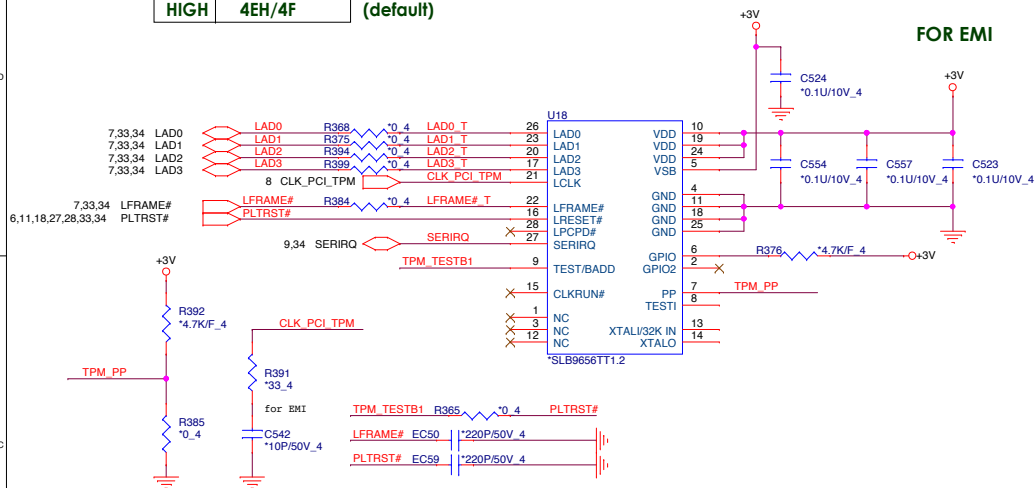
PROJECT : Y11C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	1A
Date: Wednesday, April 02, 2014	Sheet	30 of 44

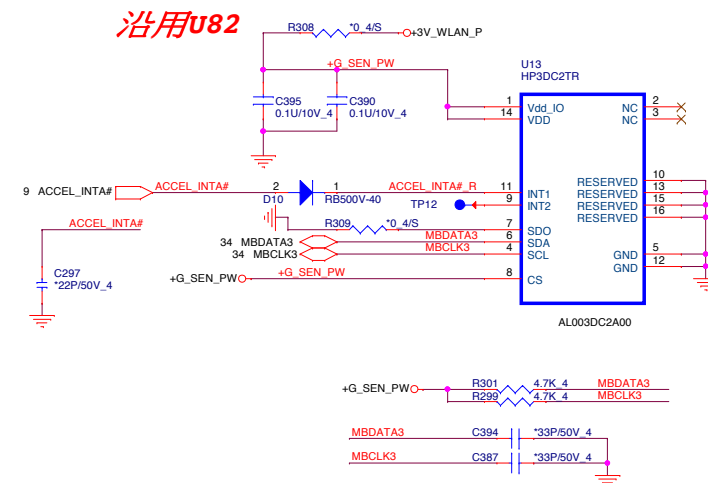
High : ODD power down
Low : ODD power on

TPM (1.2)

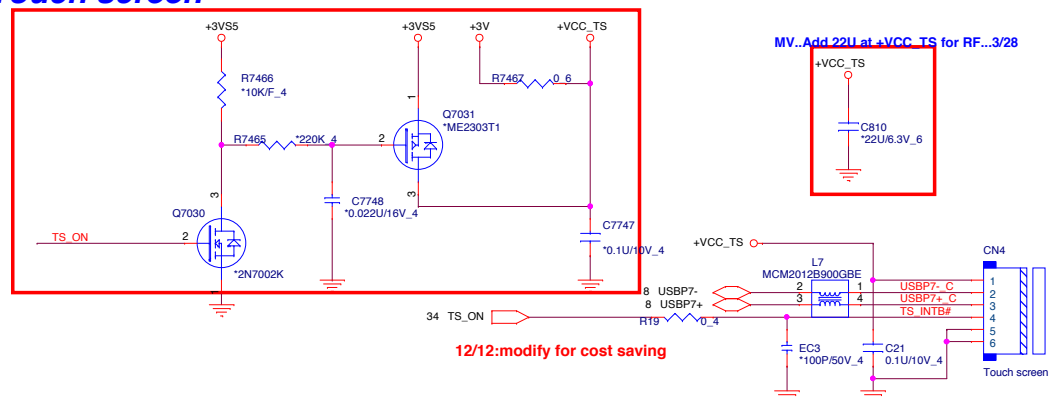
	BADD	(default)
HIGH	4EH/4F	



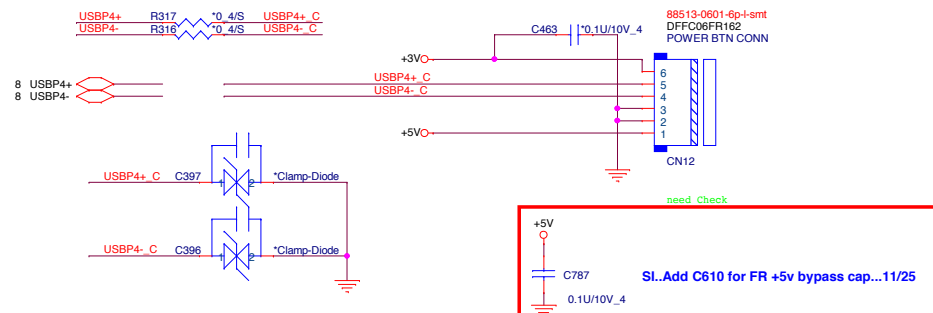
Accelerometer Sensor



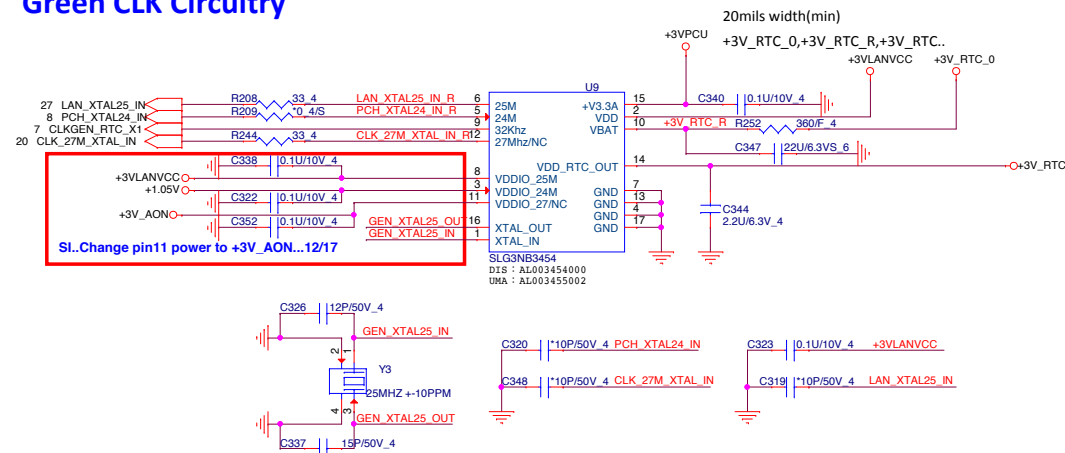
Touch screen

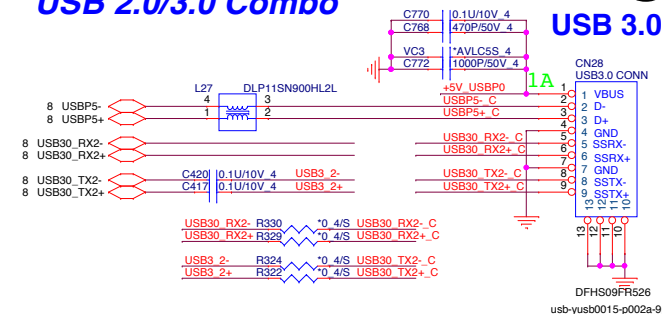


Fingerprint Conn

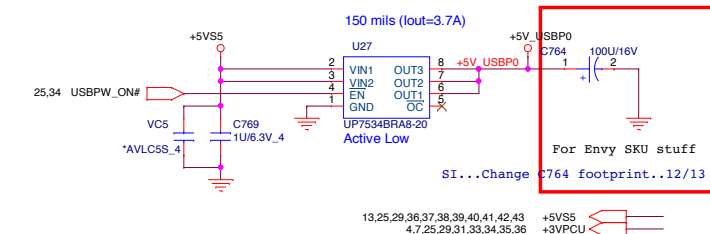


Green CLK Circuitry





The schematic diagram illustrates the USB power supply and data line connections. On the left, a +5V_USB1 input line is connected to a network of three resistors: R599 (0.8 ohms) in series, followed by R600 (0.8 ohms) in parallel with the line, and then R598 (0.8 ohms) in series. This network leads to the +5V_USB0 output line. On the right, the USBP0- and USBP0+ data lines are connected to a network of two resistors: R587 (0.4 ohms) in series, followed by R594 (0.4 ohms) in parallel with the line. This network leads to the USBP0- CHA and USBP0+ CHA lines.

[illegible]

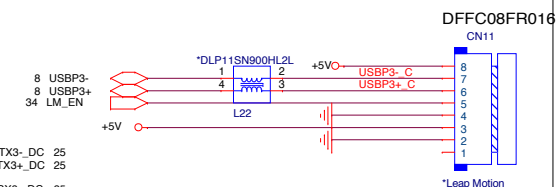
A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

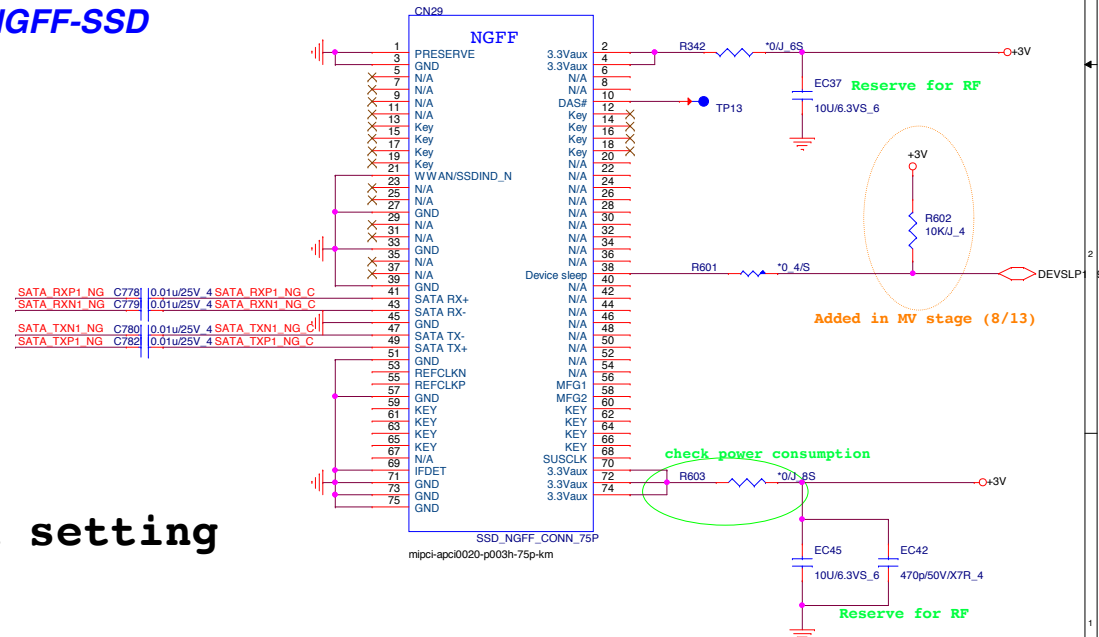
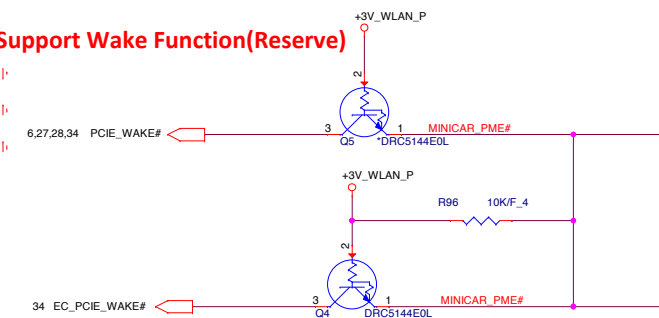
Timing diagram for the 74VHC04 hex inverters. The diagram shows the input and output waveforms for pins B, DE, and A. Each input signal is inverted at the output. The input signals are labeled B EQ0, B EQ1, B DE0, B DE1, A EQ0, A EQ1, A DE0, A DE1, and TST. The output signals are labeled R356, R361, R360, R363, R357, R362, R359, R358, and R364. The output signals are labeled with a value of 4.7K 4.

The schematic diagram illustrates the electrical connections for the USB30 module. The module's pins are numbered 1 through 34. The connections are as follows:

- USB30_TX3- (Pin 11):** Connected to C485 (0.1u/10V 4).
- USB30_TX3+ (Pin 12):** Connected to C486 (0.1u/10V 4).
- USB30_RX3- (Pin 20):** Connected to C483 (0.1u/10V 4).
- USB30_RX3+ (Pin 21):** Connected to C487 (0.1u/10V 4).
- Power Connections:**
 - +3V5S:** Connected to C491 (0.1u/10V 4) and C499 (0.1u/10V 4).
 - GND:** Connected to pins 10, 21, 25, 27, 28, 30, 31, 32, 33, and 34.
- Other Connections:**
 - USB30_TX3- DC L (Pin 11):** Connected to USB30_TX3- DC L (Pin 12).
 - USB30_TX3+ DC L (Pin 12):** Connected to USB30_TX3+ DC L (Pin 11).
 - USB30_RX3- DC L (Pin 20):** Connected to USB30_RX3- DC L (Pin 21).
 - USB30_RX3+ DC L (Pin 21):** Connected to USB30_RX3+ DC L (Pin 20).

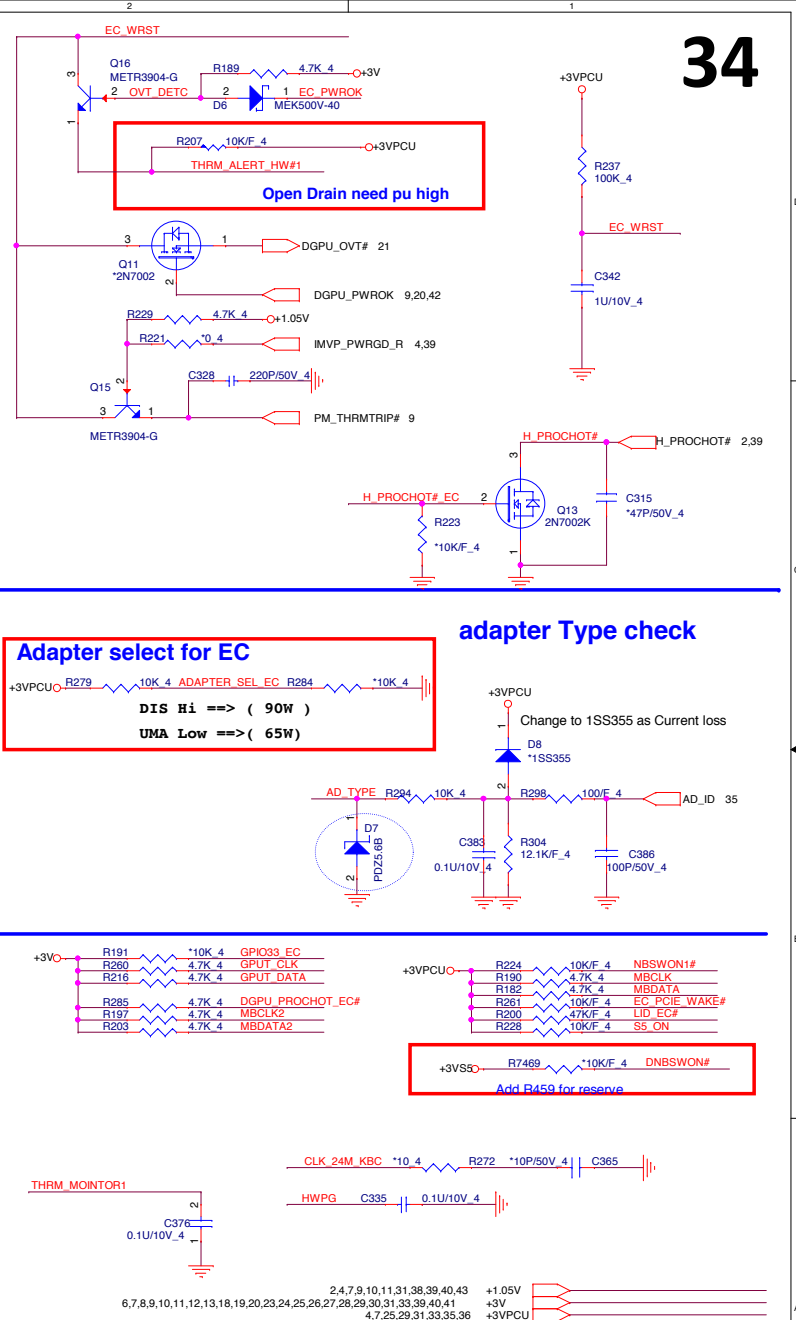
The diagram also shows a red box highlighting the connection between pins 11 and 12 of the USB30 module, and a red line connecting the TST pin (Pin 14) to the REXT pin (Pin 7) via a 5.36K resistor.





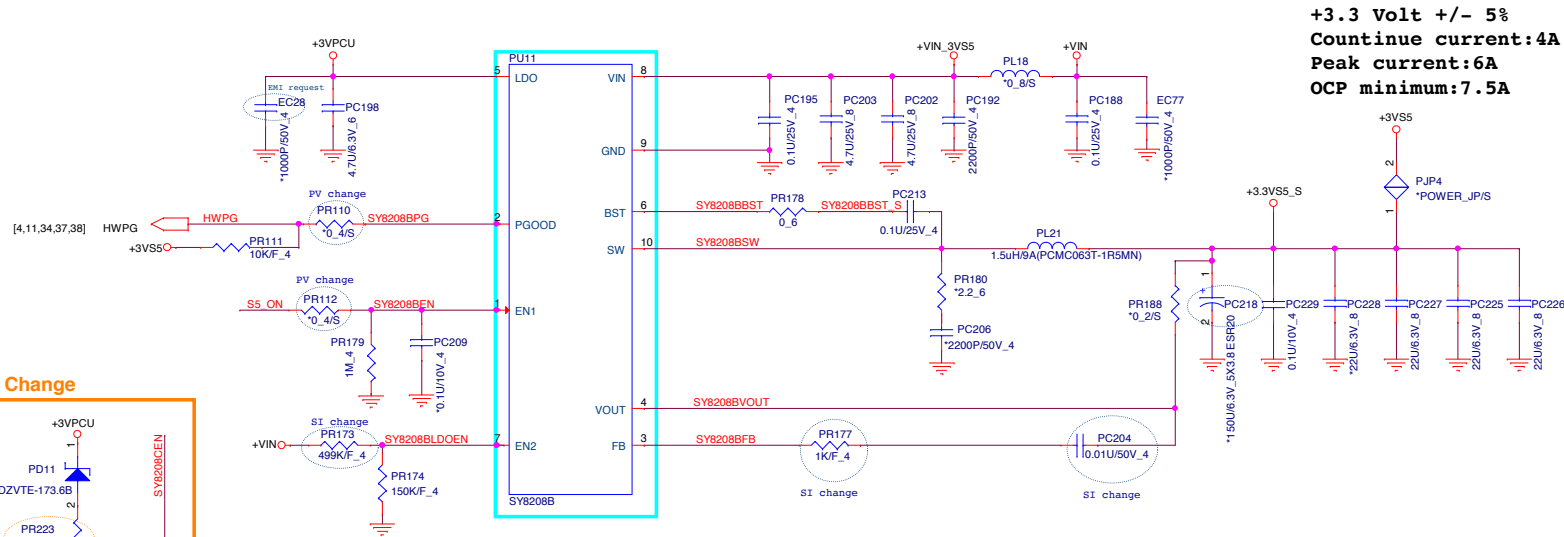
need setting

need setting

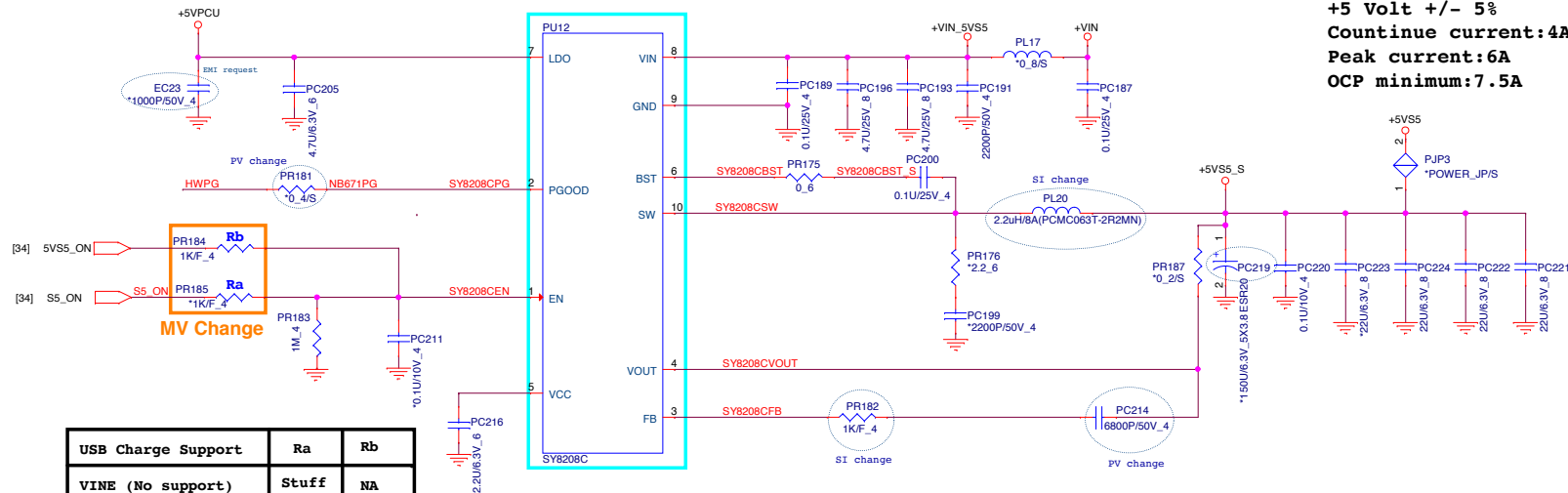
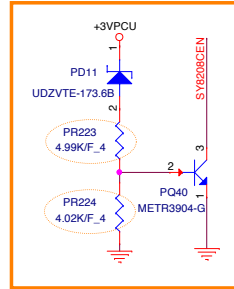




DC/DC +3VS5/+5VS5



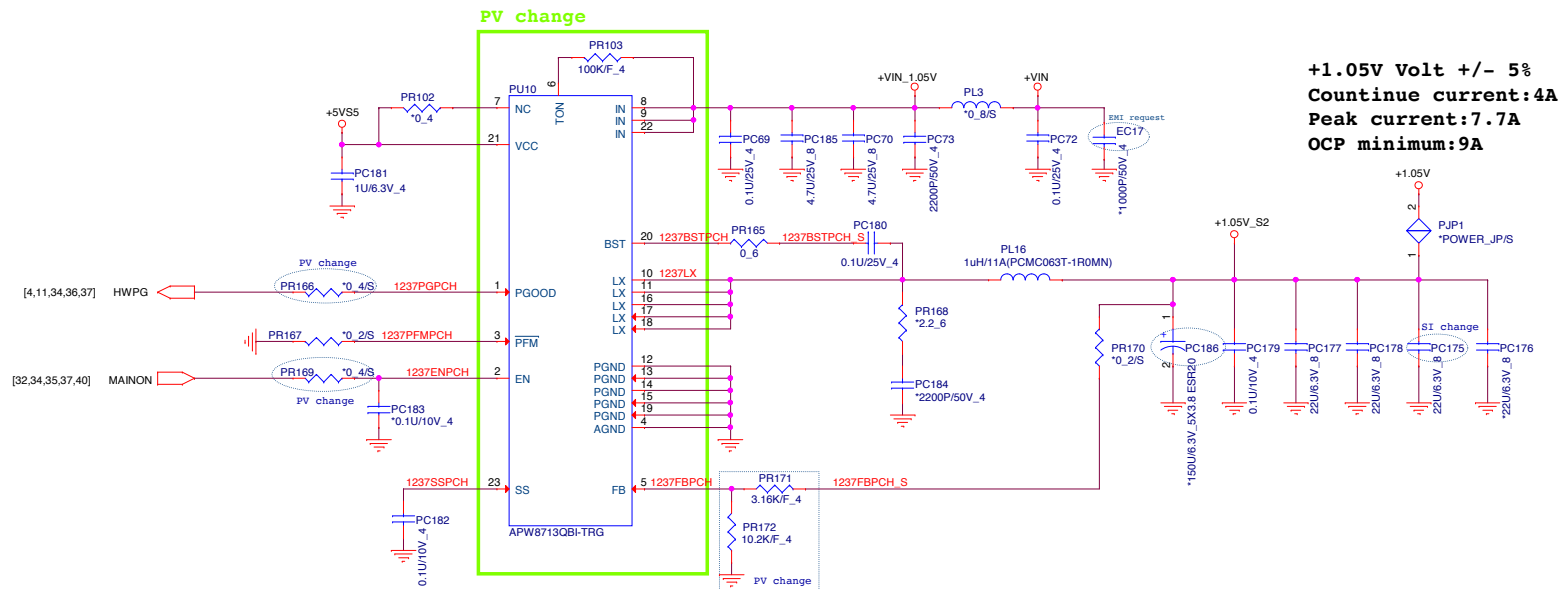
MV Change



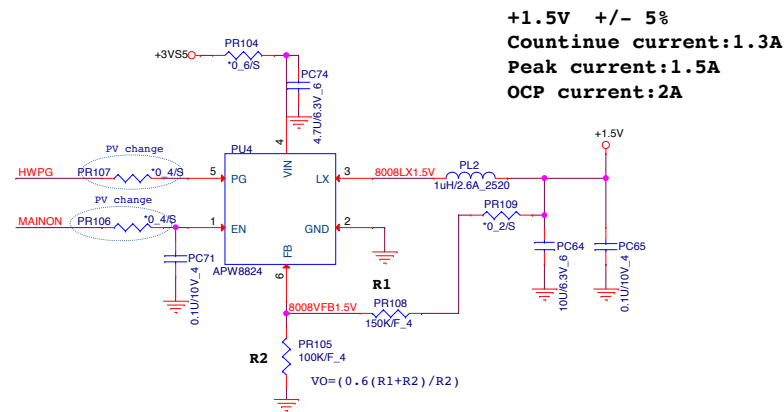
MV Change

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff




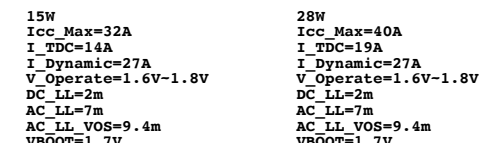


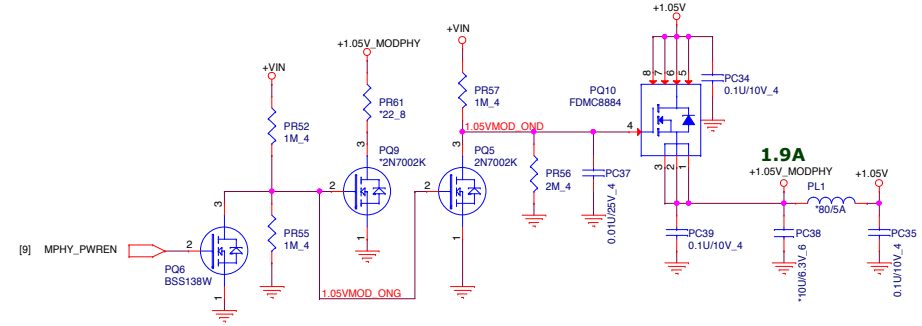
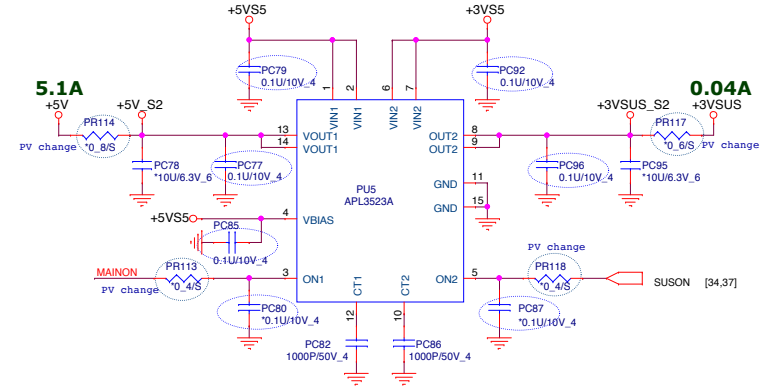
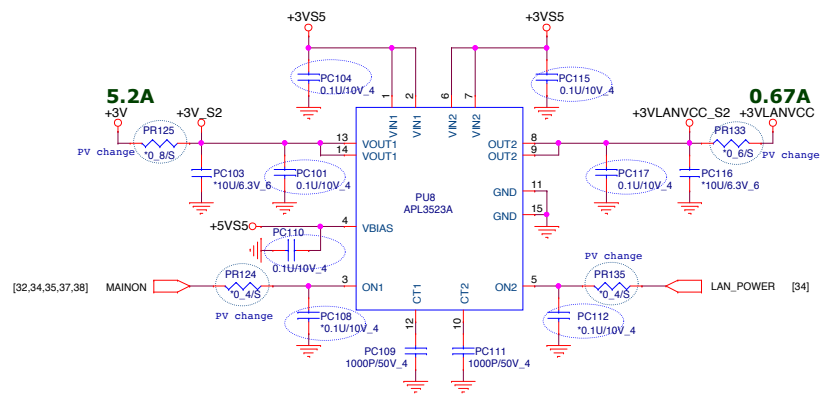
+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A



+1.5V +/- 5%
Continue current:1.3A
Peak current:1.5A
OCP current:2A


 +VIN [24,26,29,30,35,36,37,39,40,41,42,43]
 +3VS5 [6,7,9,10,11,25,29,32,33,36,40,43]
 +5VS5 [13,25,29,32,36,37,39,40,41,42,43]



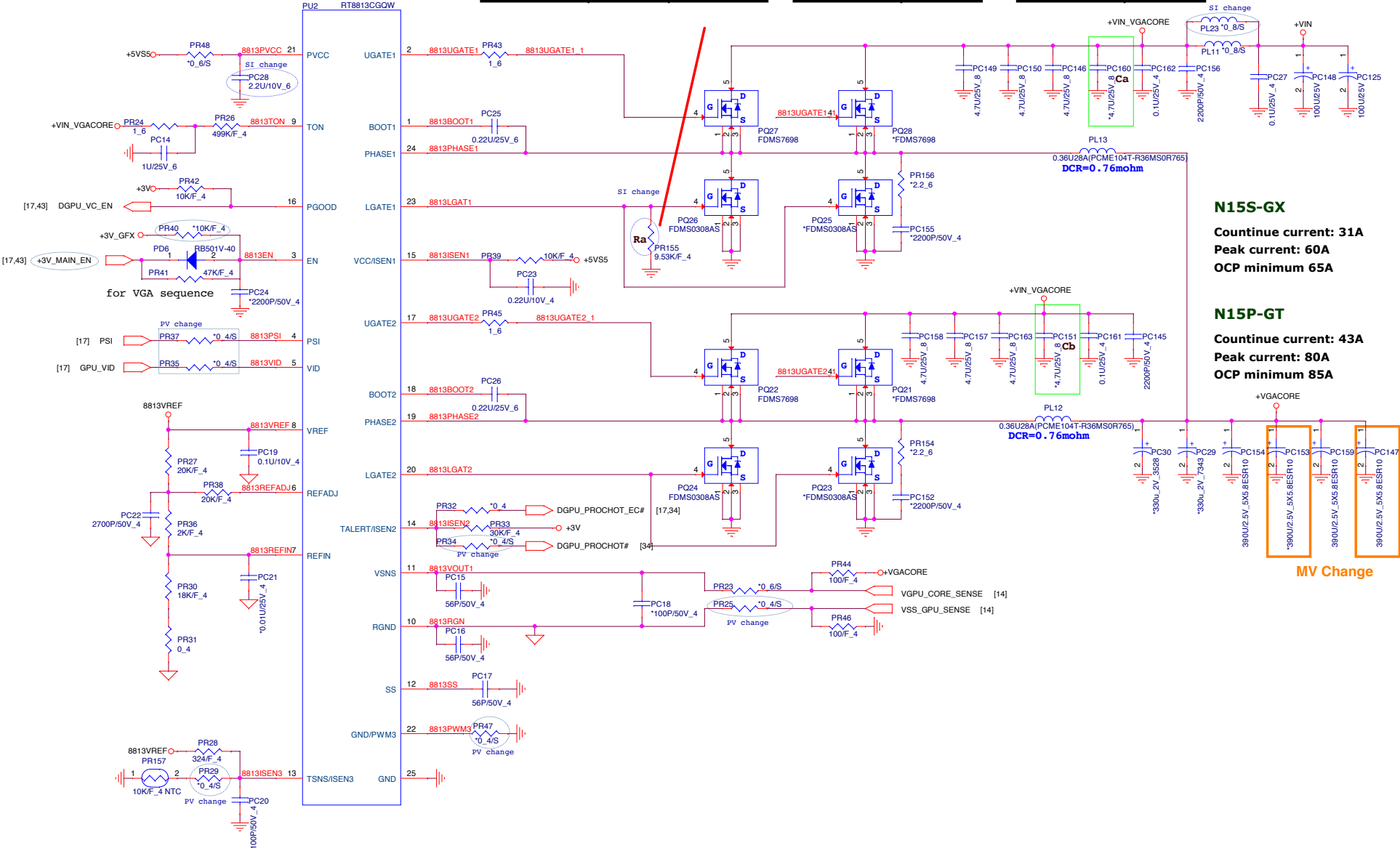


[6,7,8,9,10,11,12,13,14,17,18,23,24,25,26,27,28,29,30,31,33,34,39,41]	+3V
[24,25,26,29,30,31,32,33]	+5V
[24,26,29,30,35,36,37,38,39,41,42,43]	+VIN
[6,7,9,10,11,25,29,32,33,36,38,43]	+3VS5
[13,25,29,32,36,37,38,39,41,42,43]	+5VS5
[27,31]	+3VLAVCC

VGA TYPE	Ra Value	P/N
N15S-GX (25W)	9.53K	CS29532FB10
N15P-GT (35W)	12.4K	CS31242FB13

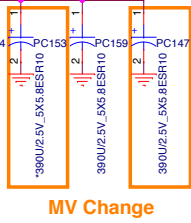
VGA TYPE	MOSFET
N15S-GX (25W)	1H1L
N15P-GT (35W)	2H2L

VGA TYPE	Ca, Cb
N15S-GX (25W)	No stuff
N15P-GT (35W)	Stuff

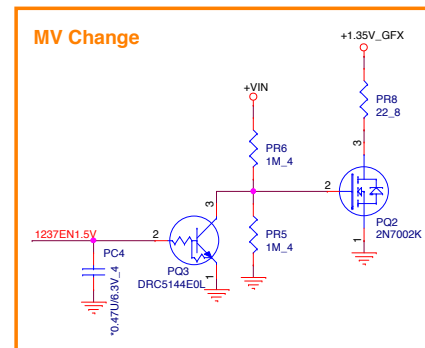
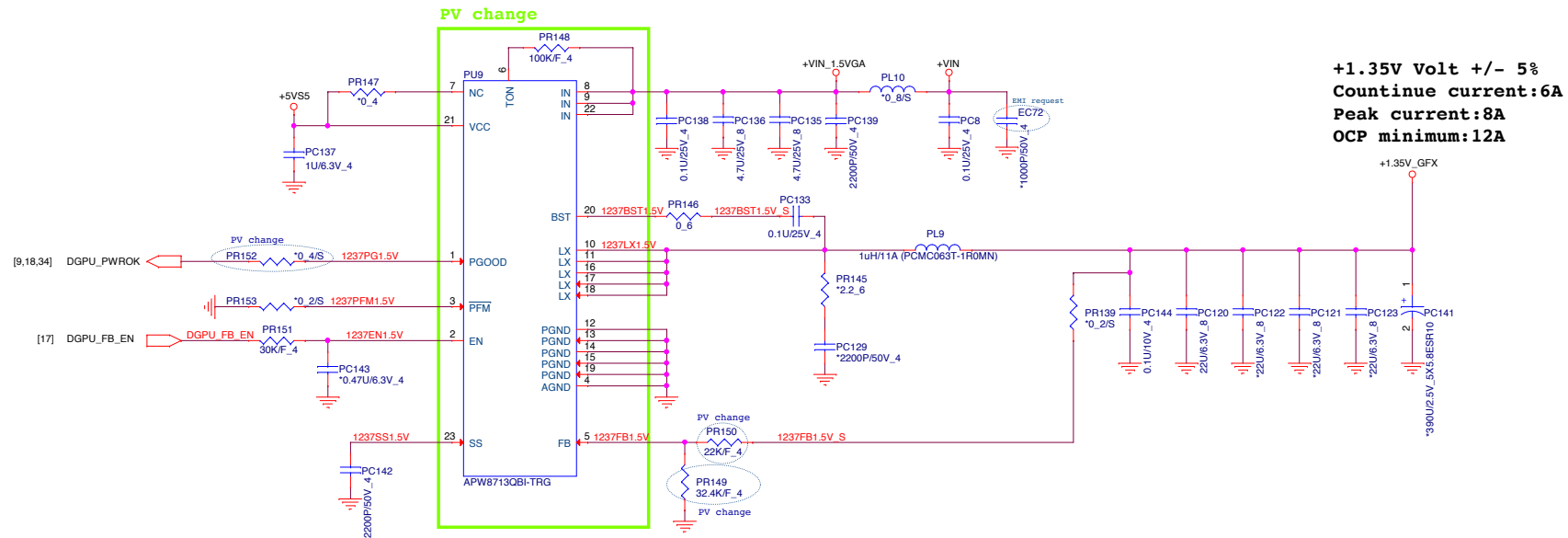


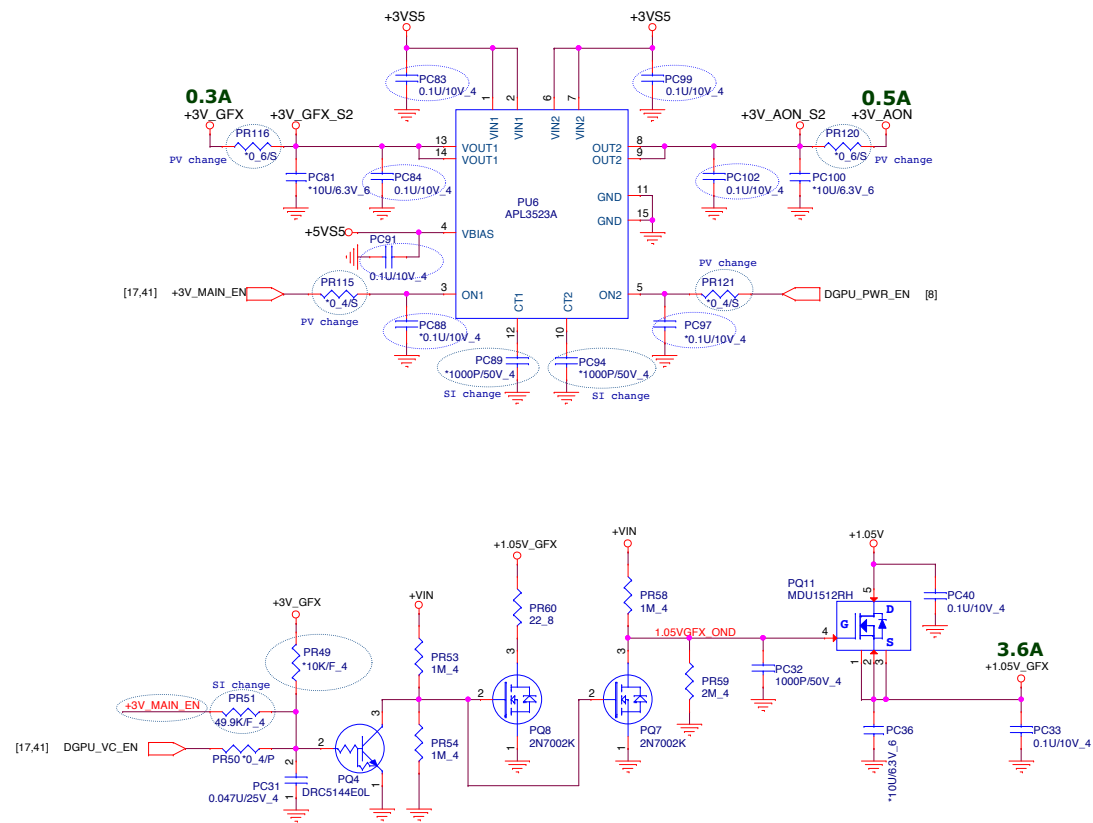
N15S-GX
Continue current: 31A
Peak current: 60A
OCP minimum 65A

N15P-GT
Continue current: 43A
Peak current: 80A
OCP minimum 85A



MV Change





Battery Connector	Pavillion	ENVY
14"	DFAD08MR063	DFAD08MR064
15"	DFAD08MR065	DFAD08MR066
17"	DFFC20FR081	DFFC20FR081

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41 、 42 、 43 ,but keep below location
Page 41	PC161 、 PC162
Page 42	PC138 、 PC144 、 PC4 、 PC148
Page 43	PC84 、 PC102 、 PC88 、 PC97 、 PC40 、 PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151 、 PC160	NA
	PQ21 、 PQ23 、 PQ25 、 PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151 、 PC160	Stuff
	PQ21 、 PQ23 、 PQ25 、 PQ28	Stuff

Title			
<Title>			
Size A	Document Number <Doc>		Rev <RevCode>
Date:	Wednesday, April 02, 2014	Sheet	44 of 44